

FRONT-END PROCESSING METROLOGY PROGRAM

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The current gate stacks, poly silicon over SiO_2 and SiON dielectrics, are being replaced by high- κ metal gate stacks. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology, and overall reliability metrology.