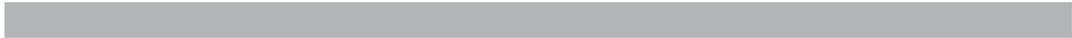


INTERCONNECT AND PACKAGING METROLOGY PROGRAM

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.



ATOMIC LAYER DEPOSITION – PROCESS, MODELS, AND METROLOGY

GOALS

Develop validated, predictive process models and *in situ* metrologies for atomic layer deposition processes.

CUSTOMER NEEDS

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high- κ gate dielectric layers, diffusion barrier layers, copper seed layers, and DRAM dielectric layers. However, significant developmental issues remain for many of these applications.

One potential solution to some ALD developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the 2003 *International Technology Roadmap for Semiconductors (ITRS)* as “one of the few enabling methodologies that can reduce development cycle times and costs.” [2003 *ITRS, Modeling and Simulation, page 1*] Important aspects of TCAD include “simulation tools that predict physical properties of materials and, in some cases, the subsequent electrical properties”; and a “hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings.” [2003 *ITRS, Modeling and Simulation, page 1*] Further, it is expected that “Simulations that can predict the impact of process conditions of film morphology as well as interface characteristics will become increasingly important.” [2003 *ITRS, Modeling and Simulation, page 15*] However, many difficult challenges to development of validated, predictive ALD process models that allow prediction of equipment influences on film properties have been identified, including “Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high- κ metal gate); reaction mechanisms, and reduced models for complex chemistry.” [2003 *ITRS, Modeling and Simulation, Table 121, page 2*] In addition to a lack of quality fundamental physical and chemical data, experimental validation has been identified as a “key difficult challenge across all modeling areas.” [2003 *ITRS, Modeling and Simulation, page 1*] Further, with respect to experimental

validation, “The major effort required for better model validation is without doubt sensor development.” [2003 *ITRS, Modeling and Simulation, page 15*] This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and associated *in situ* metrologies for ALD processes.

TECHNICAL STRATEGY

ALD process models are being developed by incorporating the detailed chemical reaction mechanisms developed in the course of this project into commercially available computational fluid dynamics (CFD) codes that simulate the flow and temperature fields in an ALD reactor. Experimental validation of the overall process model is accomplished by modeling the performance of custom-built, research-grade ALD reactors with optimized optical accessibility and benchmarking the numerical results with experimental data. These data are obtained using various measurement techniques, including vibrational spectroscopies and mass spectrometry. The focus of this work is on Al_2O_3 and HfO_2 ALD. The experimental component of this project is directed at HfO_2 ALD. However, the initial chemical mechanism development has focused on a different system: deposition of Al_2O_3 from trimethyl aluminum and water. This initial system was selected for two reasons. First, there has been significant work on Al_2O_3 ALD, and consequently, there are adequate experimental data for use in chemical mechanism validation. Second, aluminum is more amenable to quantum calculations than hafnium, a transition metal. The chemical mechanism work will be extended to the HfO_2 system, once a good understanding of detailed chemistry for Al_2O_3 ALD is developed.

This project involves two primary directions: development of *in situ* metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supporting. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that the important reaction species will be identified as the understanding of a particular ALD reaction im-

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proves, thus facilitating the design of improved process metrologies. While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, this will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetic properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

1. The first step in providing validated ALD process models is evaluating the suitability of diagnostics that are sensitive to ALD chemistry. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their potential for *in situ* monitoring. While sensors that are sensitive to gas phase species (*e.g.*, mass spectrometry and Fourier-Transform infrared (FTIR) spectroscopy) are easier to integrate into commercial reactors (*e.g.*, in the gas exhaust line), these techniques are only sensitive to volatile species. Hence, it is sometimes difficult to relate the species detected with such techniques to mechanisms of interest on the growth surface. Therefore, in addition to gas phase sensors, surface-sensitive techniques are also being evaluated to directly probe ALD surface chemistry. The suitability of Raman spectroscopy and FTIR spectroscopy for probing ALD surface processes under actual deposition conditions is being investigated. In addition, the suitability of mass spectrometry and FTIR spectroscopy for probing gas phase ALD processes and how best to relate gas phase species to important surface processes is being investigated. Research-grade ALD reactors with optimized accessibility for the various gas-phase-sensitive and surface-sensitive techniques have been designed and constructed. After various diagnostics are evaluated in these test ALD reactors, a more industrially relevant ALD reactor will be designed and built. Suitable diagnostics will be integrated into this reactor to provide data that will aid in chemical mechanism development and overall process model validation.

DELIVERABLES: Complete evaluation of *in situ* Raman spectroscopic measurements for probing ALD surface processes [3Q 2005]. Complete evaluation of *in situ* FTIR measurements for probing ALD gas phase processes [3Q 2005]. Complete evaluation of *in situ* FTIR measurements for probing ALD surface processes [4Q 2005]. Interface mass spectrometer with ALD chamber [4Q 2005].

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD and chemical vapor deposition (CVD) is an important aspect of this project and is an ongoing process. The thermochemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity compiles and evaluates currently available thermochemical and chemical kinetic data for organometallic compounds and related precursors. The second activity supplements available data by using *ab initio* and semi-empirical quantum calculations coupled with transition state calculations to develop detailed chemical kinetic models from computed molecular structures, thermodynamic properties and spectroscopic properties of relevant compounds. The third activity utilizes the experimental and computed thermochemical and chemical kinetic data to develop detailed chemical kinetic models for the decomposition of organometallic precursors and deposition processes leading to thin film growth.

DELIVERABLES: Compilation of bibliography pertaining to ALD and CVD systems. Make this information available through the Standard Reference Data website [ongoing]. Utilize and refine detailed chemical kinetic model for ALD of Al_2O_3 from trimethyl aluminum (TMA) and water based on reactor flow simulations and additional quantum calculations [3Q 2005]. Include steps in detailed chemical kinetic model to simulate carbon incorporation in Al_2O_3 ALD [3Q 2005]. Perform high level *ab initio* quantum calculations for small AlH_2X species ($\text{X}=\text{H}, \text{F}, \text{Cl}, \text{OH}, \text{NH}_2, \text{CH}_3$) to benchmark heats of formations and bond dissociation energies [3Q 2005]. Develop simple model for HfO_2 ALD from tetrakis(dimethylamino) hafnium and water [4Q 2005]. Investigate possibility of using shock tube measurements to determine bond dissociation energies of metal precursors used in ALD [4Q 2005].

3. An effort is also being made to investigate the relationship between ALD reactor conditions and concomitant HfO_2 film properties. This relationship is being investigated by correlating the results of a variety of *ex situ* film characteriza-

tion measurements to reactor conditions as determined by *in situ* measurements and numerical modeling of the temperature and flow fields in the reactor. *In situ* measurement techniques include those techniques being developed for model validation. *Ex situ* measurement techniques include vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), FTIR spectroscopy, X-ray photoelectron spectroscopy, X-ray diffractometry, and ultraviolet Raman spectroscopy. The data provided by these measurements, spatially resolved when possible, would include such film characteristics as thickness, stoichiometry, HfO₂ phases present, and degree and type of impurity incorporation.

DELIVERABLES: Complete a preliminary investigation of relationship between ALD process parameters, reactor flow and temperature fields, gas phase species identities and concentrations, and resulting ALD film characteristics [4Q 2005].

ACCOMPLISHMENTS

■ **ALD Reactor Construction** — Research-grade, optically-accessible ALD reactors have been designed and constructed with full optical access for surface and gas-phase Raman and FTIR spectroscopic measurements.

■ **HfO₂ ALD** — A pulsed gas delivery system was designed and constructed. ALD HfO₂ films were deposited under a variety of process parameters using tetrakis(dimethylamino) hafnium, Hf[N(CH₃)₂]₄, and water. Films have been characterized with a number of techniques, including VUV-SE (Fig. 1).

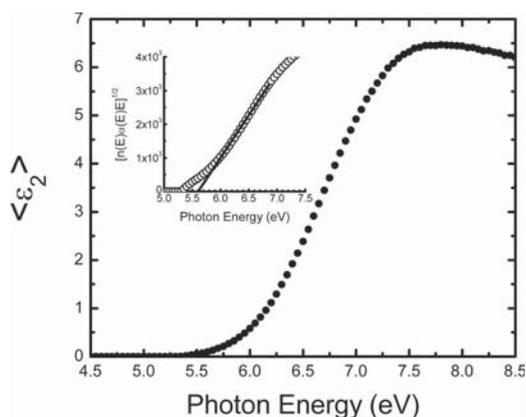


Figure 1. Imaginary part of the complex dielectric function as a function of photon energy for HfO₂ ALD film as determined using VUV-SE. The inset illustrates determination of band gap energy by extrapolation of the expression $[n(E) \cdot \alpha(E) \cdot E]^{1/2}$ to zero (data courtesy of N.V. Nguyen).

■ ***In Situ* Optical Measurements** — *In situ* surface Raman spectroscopic measurements are on going. Excitation wavelengths are being varied to evaluate maximum sensitivity to ALD species. The *in situ* gas phase and surface FTIR systems have been assembled and preliminary measurements have begun.

■ **Chemical Properties Calculations** — Molecular structures and energies for precursors, adsorbates, intermediates, and transition states have been calculated using ab initio and density functional theory quantum calculations for ALD of Al₂O₃ from TMA and water. Prototypical small cluster (Al_xO_yH_z) species have been utilized to represent the surface layer. Rate expressions based on calculated structures and energies have been derived using transition state theory (Fig. 2).

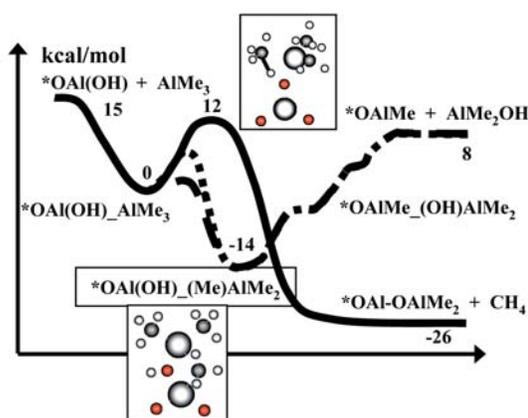


Figure 2. Calculated potential energy surface for reaction of trimethyl aluminum with a hydroxylated aluminum oxide cluster.

A detailed chemical kinetic model for ALD of Al₂O₃ from TMA and water has been constructed based on these rate expressions. This model is being refined based on further reactor model simulations, comparison with experimental observables, and supplemented with additional quantum calculations, where necessary. High level ab initio calculations, up to CCSD(T)/aug-cc-pVnZ (n=2-4) have been done for small species to benchmark heats of formation and bond dissociation energies for AlH_nX species (n = 0-2, X = H, F, Cl, OH, NH₂, CH₃). Additional calculations will be done to provide higher level corrections (e.g., core-valence, relativistic, etc).

■ **Database Website** — A Website <http://srdata.nist.gov/ckmechx/> (external) and <http://h105097.nist.gov/ckmechx> (internal) has been made available through the NIST Standard Reference

Data website. This site currently contains bibliographic and thermochemical information of silicon hydrides, halocarbons, and organometallic compounds important to semiconductor processes, including information pertaining to ALD and CVD of aluminum, Al_2O_3 , and other related ALD systems (e.g., Zr, Hf, etc.), as well as a significant amount of information pertaining to hydrocarbon-based reactions.

■ **ALD Reactor Modeling** — A two dimensional CFD model has been developed based on the dimensions of the experimental ALD reactor(s). Numerical solutions have been obtained for flow and a heated substrate with and without full chemistry for ALD of Al_2O_3 from TMA and water.

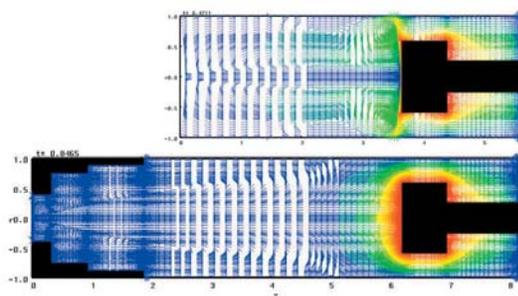


Figure 3. Two numerical simulations of the flow fields in the ALD reactor with different chamber flow geometry. Flow is from left to right. The gas temperature and velocity is represented by the color scale and vector diagrams, respectively. The top figure shows a simulation with plug gas injection and the bottom figure shows a simulation of gas injection with a conical transition region. The top figure exhibits significant gas recirculation zones while the bottom figure exhibits much more uniform flow and temperature fields.

Simulations of OH and CH_3 surface coverages agree well with experimental measurements reported in the literature. Work is ongoing in adjusting rate expressions to reproduce experimental growth rates.

■ This ALD project relies heavily on experience obtained in the course of a previous project investigating silicon thermal CVD via silane pyrolysis. That CVD project also involved development of chemical reaction mechanisms and experimental measurements to support mechanism development and process model validation. Multiple CVD process models were constructed employing the silane pyrolysis mechanisms, including gas phase nucleation of silicon particles, developed during this project and validated using the experimental results obtained in the course of this project. The

different models employed reaction mechanisms of varying complexity and reactor geometries of varying dimensionality. Experimental measurements were performed in a vertical flow, rotating disk reactor under various process conditions. Gas temperature profiles were determined using rotational Raman spectroscopy. Gas phase silicon particle spatial distributions were determined with elastic light scattering. The extent of precursor decomposition and the chemical composition of the gas-phase-nucleated particles were investigated with vibrational Raman spectroscopy. A Website (<http://www.cstl.nist.gov/div836/836.02/cvd/top-page.html>) has been established in order to disseminate the numerical and experimental results obtained from this investigation

RECENT PUBLICATIONS

J. E. Maslar and W. S. Hurst, "In Situ Optical Diagnostics of Silicon Chemical Vapor Deposition Gas-Phase Processes," *Characterization and Metrology for ULSI Technology: 2003 International Conference*, edited by D. G. Seiler et al., AIP Conference Proceedings 683, Melville, NY: American Institute of Physics, 2003, pp. 748-752.

D.R. Burgess, Jr., J.E. Maslar, W.S. Hurst, E.F. Moore, W.A. Kimes, and N.V. Nguyen, "Atomic Layer Deposition – Process Models and Metrologies," *Characterization and Metrology for ULSI Technology: 2005 International Conference*, AIP Conference Proceedings, 2005, in press.

SUPERCONFORMAL DEPOSITION COPPER AND ADVANCED INTERCONNECT MATERIALS

GOALS

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity metallizations, examining the generality of the superconformal filling mechanism and exploring processes utilizing novel barriers and/or seed geometries.

CUSTOMER NEEDS

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to “superconformally” fill high aspect ratio features has made electrodeposited copper the interconnect material of choice in silicon technology. However, the move to ever smaller dimensions has led to the rise of new challenges, including fabrication of ever thinner copper seeds that are required for the copper superfill process and increased resistivities of the metallizations due to size effects. To overcome these hurdles the National Institute of Standards and Technology (NIST) has a program focusing on new fabrication techniques such as seedless processing, and evaluation of the factors affecting electrical resistivity of sub-100 nm wires as well as enhancing existing copper technology through improved understanding of the fundamentals of the superfill process.

Interconnect metallization issues are discussed in the Interconnect section of the 2004 update of the International Technology Roadmap for Semiconductors

TECHNICAL STRATEGY

To meet future industrial needs, we have developed the metrology and fully disclosed copper electrolytes that permit characterization of the ability of generic electrolytes to fill fine features. We have also developed electrolytes and metrology for superconformal deposition of advanced interconnect materials such as silver (the only metal with a higher conductivity than copper) and gold (metallization for compound semiconductors) as well as alternative processing schemes such as chemical vapor deposition (Fig. 1A).

Current metallization technology employs three layers, a barrier metal, typically tantalum, a PVD copper seed and electrodeposited copper. As feature sizes continue to shrink the resistive barrier materials may account for an increasing portion of the cross-sectional area and thus negatively impact electrical performance. These difficulties have driven a search for alternative barrier materials and processes. Ruthenium is a particularly attractive candidate because its electrical and thermal conductivities are approximately twice those of conventional tantalum barriers and ruthenium and copper are immiscible. Substitution of a noble metal barrier/seed layer for the current Ta/Cu technology promises the combined advantages of process simplification and enhanced performance.

Our preliminary work in this area revealed an interesting sensitivity of trench filling behavior to the manner in which the ruthenium barrier layer was treated prior to plating.

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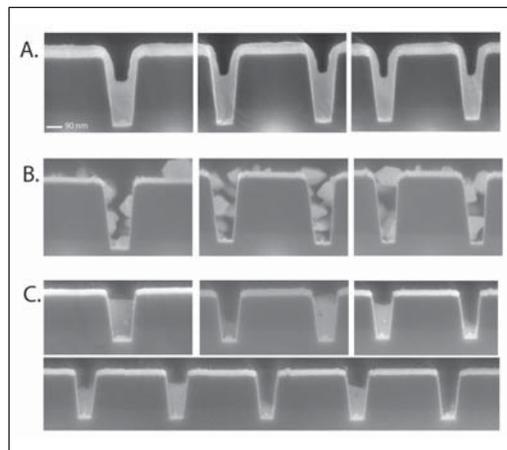


Figure 1. Nucleation and growth of copper on ruthenium is a sensitive function of the initial surface state. Three limiting behaviors are shown: A. Exemplifies the desired result, namely, early coalescence of the electrodeposited copper followed by superfilling that is characteristic of growth on conventional a copper seed-layer; B. Volmer-Weber growth mode characteristic of poor copper wetting on oxidized ruthenium and consequently poor trench filling; and C. Selective growth within the feature that is observed sporadically in a few specimens.

DELIVERABLES: Publications detailing copper superfilling directly on ruthenium barriers (2Q 2005).

A clear understanding of these observations will be required to establish a robust manufacturing process. Voltammetry is a particular powerful tool for examining the surface state of ruthenium and the effect of various surface pretreatments on superfilling behavior. As shown below (Fig. 2), a two-dimensional wetting layer or “underpotential deposited copper” rapidly forms on a ruthenium surface that is first activated by reduction at negative potentials. In contrast, on an oxidized ruthenium surface copper deposition proceeds by the undesirable Volmer-Weber growth mode and poor trench filling results (e.g., Fig. 1B).

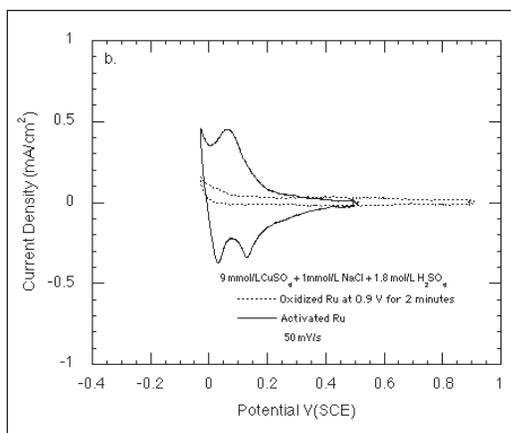


Figure 2. The deposition and stripping of a 2-D copper layer on an oxide-free ruthenium surface. Oxidation of ruthenium at high potentials inhibits this process with negative consequences for morphological evolution during bulk copper deposition as well as poor interfacial adhesion.

As feature widths and seed-layer dimensions decrease a move to Atomic Layer Deposition (ALD) of the barrier layer is anticipated. Successful process integration will require close control of the surface chemistry of the barrier and consideration of the terminal effect (potential drop associated with highly resistive seed-layer) and the consequences of potential-dependent morphological evolution during copper electroplating. Formative steps examining these issues are underway in collaboration with the University of Helsinki (Fig. 3).

DELIVERABLES: Publication on seedless trench superfilling of copper directly deposited on ALD barrier layers. (4Q 2005).

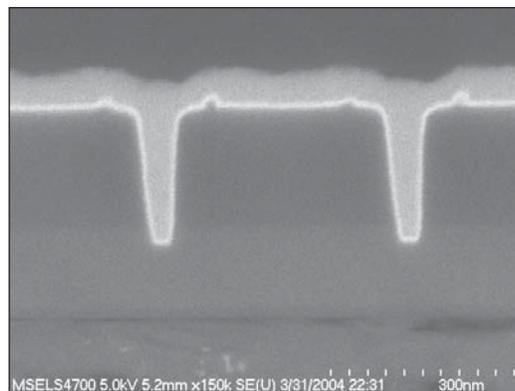


Figure 3. Trenches superfilled with copper electrodeposited directly on an ALD iridium layer (thin bright layer).

A new effort this year focused on exploring gold metallization for III-V semiconductors such as GaAs and GaN. In analogy to silicon technology the push to higher device density may require a move to Damascene processing of compound semiconductors. The first demonstration of void-free bottom-up filling of trenches by gold electrodeposition was recently published by NIST. Further work is underway to quantitatively describe the process (Fig. 4).

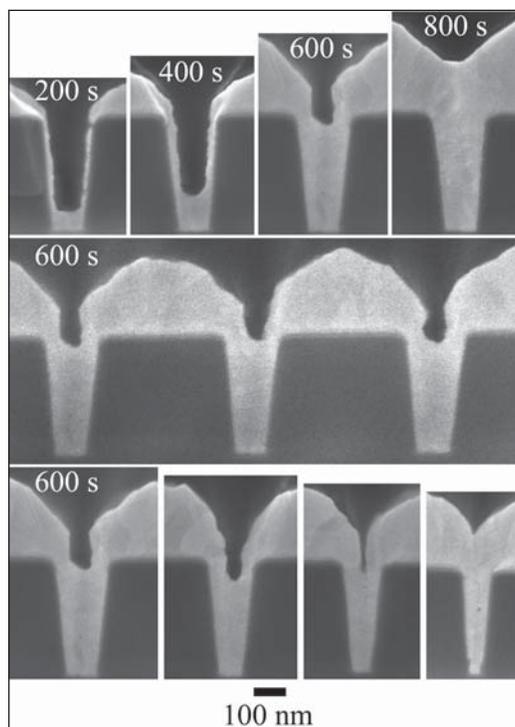


Figure 4. Void-free filling of trenches with gold. The gold seeded substrates were first derivatized with a sub-monolayer of lead followed by electrodeposition in gold cyanide electrolyte for the times shown.

DELIVERABLES: Publication detailing void-free trench filling with gold (2Q 2005).

One of our newest publications extends our Curvature Enhanced Accelerator Coverage (CEAC) mechanism to include the impact of catalyst consumption. While such consumption degrades superfilling ability of the electrolyte, and leads to undesirable incorporation of impurities in the deposit, it is a very real phenomenon.

DELIVERABLES: Published two invited papers; IBM Journal of Research (2Q 2005) and The Electrochemical Society's news journal Interface (1Q 2005). These papers present a synopsis of the substantial output of the NIST superfill effort to the most relevant industrial audience.

Further surface analytical and electroanalytical experiments are underway to provide a deeper understanding of competitive dynamics between multicomponent adsorption, consumption and the connection with microstructural and morphological evolution.

DELIVERABLES: Present the first study that uses surface analytical probes to quantify the coverage of active surfactants for comparison with the predictions of the CEAC mechanisms derived from electroanalytical kinetic measurements (4Q 2005).

Theoretical and experimental work is also underway to probe the coupling of the CEAC mechanism with the traditional diffusion-adsorption-consumption model of leveling. The robust modeling of the competitive dynamics between catalytic brightener and poisoning leveling additive represent one of the current strategies employed by industry to circumvent the negative effects of bump formation (also called "momentum plating") that hampers conventional post-plating planarization technologies. A new code has been developed that details the effect of competition between a suppressor, catalyst, and leveler for surface sites and the subsequent effect on metal deposition and shape change. The code operates on the freeware Python platform, to ensure greater access, and to be more efficient and user friendly. The code has been downloaded by research groups around the world.

DELIVERABLES: Develop and make available advanced software for modeling superconformal filling of vias and trenches. The (3Q – 4Q 2005).

ACCOMPLISHMENTS

We have demonstrated void-free bottom-up filling of trenches with gold that may find use in

the formation of contacts and metallizations for compound semiconductors.

We have demonstrated the use of ruthenium barriers to obtain superconformal electrodeposition of copper metallizations without the need for a copper seed layer. Established metrics for effective seedless superfill.

Developed a protocol for quantifying the kinetics of catalyst consumption on the electrodeposit surface and the (detrimental) impact of such consumption on the superconformal feature filling process.

COLLABORATIONS

D. Wheeler, R.R. Keller, Y.-W. Cheng, J.E. Bonevich, D.R. Kelley, L.J. Richter, M.L. Walker, W.F. Egelhoff, J. Mallett, G.B. McFadden, S.R. Coriell, NIST.

International SeMaTech, Christian Witt; fabrication of patterned substrates with electrical test structures including sub-100 nm wire widths.

T. Aaltonen and M. Ritala, University of Helsinki; ALD deposition of Ru and Ir seed layers.

Clarkson University, Y. Li and C. Burkhard; chemical mechanical planarization of electrical structures.

RECENT PUBLICATIONS

D. Josell, C.R. Beauchamp, D.R. Kelley, C.A. Witt and T.P. Moffat, "Gold Superfill in Sub-Micrometer Trenches," *Electrochem. & Solid-State Lett.* 8, C54 (2005).

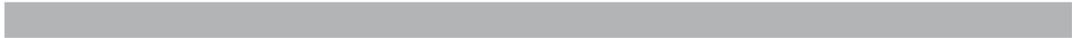
T.P. Moffat, D. Wheeler, M. Edelstein and D. Josell, "Superconformal Film Growth: Mechanism and Quantification," *IBM Journal of Research* 49, 19 (2005).

T.P. Moffat, D. Wheeler and D. Josell, "Superfilling and the Curvature Enhanced Accelerator Coverage Mechanism," *Interface* 13, 46 (2004).

D. Wheeler, T.P. Moffat, G.B. McFadden, S. Coriell and D. Josell, "Influence of Catalytic Surfactant on Roughness Evolution During Film Growth," *Journal of the Electrochemical Society* 151, C538 (2004).

T.P. Moffat, D. Wheeler, and D. Josell, "Electrodeposition of Copper in the SPS-PEG-Cl Additive System: I. Kinetic Measurements: Influence of SPS," *Journal of the Electrochemical Society* 151(4), C262-C271 (2004).

D. Josell, C. Burkhard, Y. Li, Y.-W. Cheng, R.R. Keller, C.A. Witt, D. Kelley, J.E. Bonevich, B.C. Baker, T.P. Moffat, "Electrical Properties of Superfilled Sub-Micrometer Silver Metallizations," *Journal of Applied Physics* 96, 759 (2004).



NANOPOROUS THIN-FILM METROLOGY FOR LOW- κ DIELECTRIC MATERIALS

GOALS

In this project, we are developing measurement methods of the structure and properties of nanoporous thin films for low- κ dielectric applications. We work closely with industrial collaborators to develop and apply these methods to advanced materials destined for integration in the next generation of integrated circuits. The unique measurement methods we apply include X-ray reflectivity (XR), small angle neutron scattering (SANS), Rutherford backscattering spectroscopy (RBS), and forward recoil elastic spectroscopy (FRES). Our efforts focus on two areas, providing high quality data and measurements of film thickness, coefficient of thermal expansion (CTE), moisture uptake, film connectivity, pore volume, pore size, and matrix density on films under development, and devising new measurement methods to characterize pore size distribution (PSD), pore connectivity, and matrix homogeneity.

CUSTOMER NEEDS

As integrated circuit (IC) feature sizes continue to shrink, new low- κ interlevel dielectric materials are needed to address problems with power consumption, signal propagation delays, and cross talk between interconnects. One avenue to low- κ dielectric materials is the introduction of nanometer scale pores into a solid film to lower its effective dielectric constant as discussed in 2004 ITRS, Interconnect, pages 1 and 2. However, the pore structure of these low- κ dielectric materials strongly affects important material properties other than the dielectric constant such as mechanical strength, moisture uptake, coefficient of thermal expansion, and adhesion to different substrates. The characterization of the pore structure is needed by materials engineers to optimize and to develop future low- κ materials and processes. Currently, there is no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates include silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. With the large number of possible materials and processes, there is a strong need for high quality structural data to understand correlations between processing conditions and the resulting physical properties.

TECHNICAL STRATEGY

■ The small sample volume of 1 μm films and the desire to characterize the film structure on silicon wafers narrows the number of available measurement methods. A unique suite of measurement techniques, Fig. 1, has been developed at NIST using a combination of SANS, XR, RBS, and FRES to determine important structural and physical property information about thin porous films less than 1 μm thick deposited on a 1 mm thick substrate. These measurements are performed directly on films supported on silicon substrates so that processing effects can be investigated.

The elemental composition of the films is determined by RBS for silicon, carbon, and oxygen and FRES for hydrogen. In both techniques, a beam of high-energy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy. Fits are performed on the scattered peaks to compute the relative fraction of each element. The atomic composition information is necessary to calculate the relative contrast factors for X-rays and neutrons.

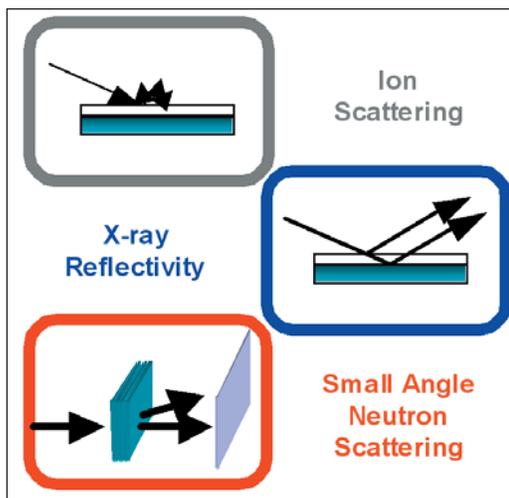


Figure 1. Three thin film measurements that are combined for complete characterization.

The XR experiments are performed at grazing incident angles on a modified to θ - 2θ X-ray diffractometer at the specular condition. With the modified configuration, reflectivity fringes

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Wen-li Wu

“The SANS/SXR measurements have become a key metric in our low- κ dielectric materials characterization and screening process”

Jeffrey Wetzel –
International SEMATECH

“The NIST X-ray reflectivity program is useful, perhaps even critical, to the industry”

Abner Bello –
Applied Materials

can be observed from films up to 1.2 μm thick. High-resolution XR is a powerful experimental technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. In addition, changes in the density profile from processing or post-application treatments can be determined. The CTE is determined from measurements of the film thickness at different temperatures.

The SANS measurements are performed at the NIST Center for Neutron Research (NCNR). Up to 10 films are stacked to increase the SANS signal and the samples are placed in vacuum without any obstructions between the sample and the neutron detector. Scattering measurements are initially performed under ambient conditions to determine the structural characteristics of the pore structure. The scattering data are initially analyzed using a simple random two-phase description of the film, the Debye model. This model is appropriate for a class of films having random pores that makes up a majority of the samples measured. Other models are applied where appropriate such as a polydisperse collection of non-overlapping spherical pores. An additional method has been developed in which the Debye model is extended to include more complex distributions of pore sizes that need not be spherical in shape.

DELIVERABLES: Measure and report on up to 20 films for pore volume, pore size, and matrix density associated with ISMT. 3Q 2005

■ Further developments in the determination of pore size distributions have focused on the adaptation of conventional probe molecule porosimetry methods to the NIST experimental techniques. For example, XR was done on films that have been measured in vacuum in a conventional way, and then exposed to saturated toluene vapor for several hours (Fig. 2). Capillary action fills the pores of the film. The XR critical edge where adsorption first begins gives an accurate value of the average mass density that is a combination of the walls and the solvent-filled pores. By comparing the results of the sample in air or vacuum with the toluene adsorbed, one can calculate the amount of toluene adsorbed, and hence the volume of open pores. Also, XR oscillations at higher angles provide a measurement of the total film thickness before and after exposure to toluene and give a measure of

the solvent resistance of the material and rigidity of the walls.

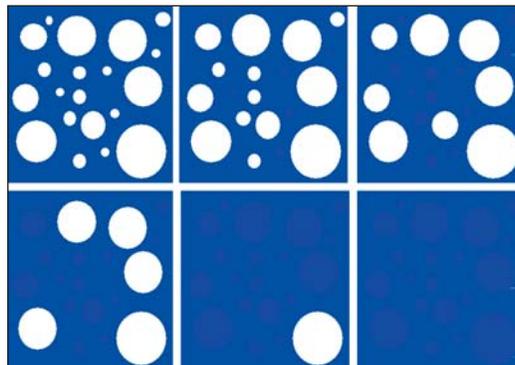


Figure 2. Schematic of the porosimetry measurement, increased solvent vapor pressure fills increased pore sizes.

The toluene infusion results confirm that the open pores of thin films can be filled by toluene supplied by saturated vapor and that XR can accurately measure the amount adsorbed. If the vapor pressure of the toluene or any other condensable solvent can be controlled at a partial pressure, standard porosimetry techniques may be applied to thin films. Data on the amount of solvent adsorption for a series of pressures could be converted to a PSD through the appropriate thermodynamic analysis.

DELIVERABLES: Publish Recommended Practice Guide for X-ray Reflectivity: X-ray Porosimetry for distribution to interested parties. 4Q 2004

■ The use of deuterated and hydrogenated probe molecules enables the powerful use of contrast match methods with the SANS technique. This technique can be used for characterization of the porous thin films by filling the pores with various mixtures of toluene- h_8 and toluene- d_8 . If the pores are accessible to the solvent and there are homogeneous walls, the wall density can be found. If the wall is heterogeneous, the average wall density could be found with information on the extent of heterogeneity also being possible. If closed pores exist that are inaccessible to solvent, closed pore porosity can be determined.

We have developed a combination of contrast match SANS and XR porosimetry. A match solvent mixture at controlled vapor pressures deposits the contrast match liquid in the pores through capillary action. SANS would provide an additional measure of PSD.

DELIVERABLES: Develop measurement methods for SANS contrast match porosimetry technique. 1Q 2005

ACCOMPLISHMENTS

■ We continue to work with SEMATECH (SMT) on a project in which 20 thin films have been characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and distributed to member companies. Additional measurements were performed on specific samples for further analysis using methods such as additional SANS configurations or X-ray porosimetry.

■ A NIST special publication was released that provides details of recommended practice guidelines for the use of X-ray porosimetry for the characterization of nanoporous thin films. X-ray porosimetry measurements were developed utilizing the controlled infusion of toluene into the open pores of a film through mass flow controllers and computer control. All of the connected open pores become filled with liquid toluene through capillary action. The critical edge measured by XR is used to calculate the total mass density and, hence, the total amount of adsorbed solvent and open pore content. This method allows calculation of the total open pore porosity that can be compared to the total combined open and closed pore porosity that is measured by the previous method that uses a combination of XR, SANS, RBS, and FRES. Further, pore size distributions may be extracted using conventional thermodynamic equations from obtained absorption/desorption curves.

■ A contrast match method using saturated solvent vapor was developed to provide an independent SANS measurement of pore volume, pore size, and matrix density as well as pore connectivity, and matrix homogeneity. The films in the SANS cell become saturated by the vapor and the pores become filled. Several solvent ratios are used and the SANS results of the saturated films along with SANS of the films in vacuum are used to calculate the exact match composition. The match composition is used to calculate the mass density of the matrix material and closed pores. This matrix density measurement is independent of the method that uses toluene infusion XR. The contrast match method offers improved accuracy of the final measured parameters. The matrix heterogeneity and the closed pore content can also be determined by the contrast match method.

The contrast SANS method was further advanced by performing SANS porosimetry measurements to determine pore size distributions that may be compared with the X-ray porosimetry data.

■ The structural evolution of pore formation in low- κ dielectric thin films (with a deuterated porogen) at various stages in processing was investigated using a combination of specular X-ray reflectivity (SXR) and small angle neutron scattering (SANS). SXR provides information as to the porosity and the density of the wall. SANS data show that the neutron scattering decreases during processing as the deuterated porogen degrades and pores are formed. The pore size and pore size distribution were estimated by fitting the SANS data to a structural model that describes the scattering intensity from a population of polydisperse spheres that includes hard sphere interactions between the particles and uses a Schultz distribution to describe the polydispersity. The porosity was found to decrease, while the pore size increased, during processing. A practical method of transforming phase size distributions into density correlation functions has been demonstrated. The computations are rapid and can produce density correlation functions, and hence scattered intensities to any necessary degree of accuracy. Phase size distributions other than the exponential ones described by Debye *et al.* can be transformed into density correlation. The transformation of scattered intensity into model phase size distributions is possible by this method.

■ Initial feasibility studies have demonstrated the potential of Small Angle X-ray Scattering (SAXS) to detect and to estimate the extent of sidewall damage of nanoporous low- κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low- κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ , it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low- κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low- κ material, then backfilled the trenches with the same candidate low- κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays.

DELIVERABLES: Determine feasibility of SAXS measurement methods for sidewall damage characterization in plasma etched patterned low- κ dielectric materials. 4Q 2005.

COLLABORATIONS

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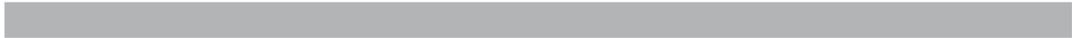
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INTERCONNECT MATERIALS AND RELIABILITY METROLOGY

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in two sub-sections, each focusing on a single aspect. These are:

- Basic Materials Properties
- Interconnect Test Structures



BASIC MATERIALS PROPERTIES

GOALS

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin interconnect conducting and insulating films, including basic tensile properties, elastic modulus by both static and dynamic means, residual stresses, fatigue, fracture resistance, and electromigration and stress-voiding resistance, in specimens fabricated and sized like materials used in actual commercial devices; and (2) to advance the ability to anticipate and meet thin interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of thin film failure, for example, electromigration and mechanical fatigue.

CUSTOMER NEEDS

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 10 thin-film layers now, and will soon reach 12 layers (*International Technology Roadmap for Semiconductors, 2004, Interconnect, Table 81a*). These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low- κ dielectric, and operate at ever higher temperatures. Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the *Roadmap (2003, unchanged for 2004), Interconnect, p. 34, Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. The 2003 NEMI (National Electronics Manufacturing Initiative) Research Priorities document reports a similar need. In a section beginning on page 24, entitled Modeling, Simulation and Design Tools, Emerging Areas for Electronics Packaging, Table 3, Projected Development and Research Needs for Simulations in Emerging Areas, in-*

cludes nanoscale modeling and simulation as an area, experimental tools capable of measuring electrical, thermal, and mechanics phenomena/material properties at smaller scale as a need, and "Issue: how is the property and behavior different from bulk behavior/macro-scale?" as a comment. The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets.

Because the films are formed by physical vapor deposition or spin-on deposition, their microstructures, and hence their mechanical properties, are quite different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset, to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology. We held a workshop entitled Reliability

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Issues in Nanomaterials, 17–19 August 2004, to gauge customer interest in the available tools for characterization of nanomaterials, which, of course, encompasses advanced interconnect structures at both current and foreseen size scales. Microelectronics manufacturers were represented, along with universities, national laboratories, and more general commercial interests.

DELIVERABLE: Report, 2Q 2005, on workshop: Reliability Issues in Nanomaterials, held August 17–19, 2004.

The report to be published in 2005 gives the details, but two key messages for this research project were the widespread adoption of nanoindentation for material characterization, and the serious consideration given to atomic-scale materials engineering.

TECHNICAL STRATEGY

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand.

We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1). Oc-

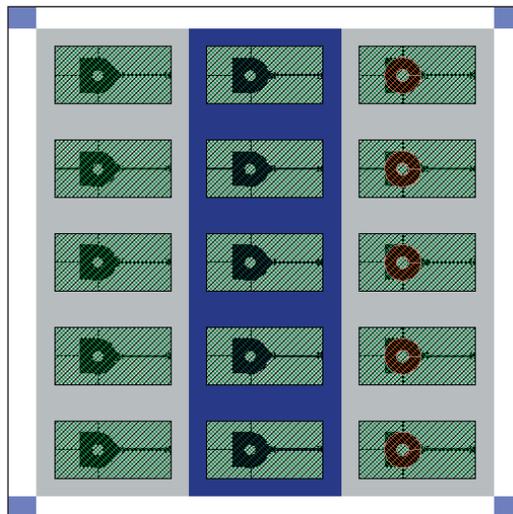


Figure 1. Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

asionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry.

DELIVERABLE: Microtensile test results on a new variety of electrodeposited copper will be reported to an industry collaborator, 2Q 2005

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. thermomechanical fatigue measurements, and resonant structure measurements. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. Because problems were encountered with specimens narrower than 100 μm , a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the scanning electron microscope (SEM). This system has now been used on specimens as small as 2 μm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

We have begun an effort on electrodeposited copper, including specimens from industrial colleagues and produced in-house, to characterize the variability of the mechanical behavior of electrodeposited copper with deposition conditions, film thickness, annealing, and other relevant variables.

Our measurements involving alternating current stressing of chip-level interconnects are used to explore the relationships between electrical and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in the lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material. The use of advanced analytical techniques including electron back scattering diffraction (EBSD) and transmission and scanning electron microscopy (SEM and TEM) has revealed surprisingly similar microstructural damage and failure mechanisms in a.c.-stress and microtensile tests. This indicates at least the possibility that electrical tests may be exploited to produce information about the mechanical

characteristics of thin films. If this electrical-mechanical test can be made to produce relevant data, it will be of significant benefit because of the experimental convenience of electrical stressing on specimens of a wide range of sizes, including very small.

We have work in progress, with the NIST Metallurgy Division, to address reliability of advanced interconnect materials with linewidth less than 100 nm. In addition to the challenges associated with electrodeposition into extremely narrow trenches, we expect significant influences of the interconnect sidewalls on electrical resistivity and possibly on thermomechanical fatigue resistance.

We are also developing non-contact optical methods to measure mechanical properties of thin films and interconnects using MEMS test structures that are compatible with the CMOS process. Such non-contact methods may be useful in monitoring the variations of mechanical properties in the production environment. A method has already been developed to measure the residual strain in the passivation and interconnect films using fixed-fixed beams. We are currently developing resonant measurements for cantilever beams to characterize the elastic modulus of each layer (Fig. 2).

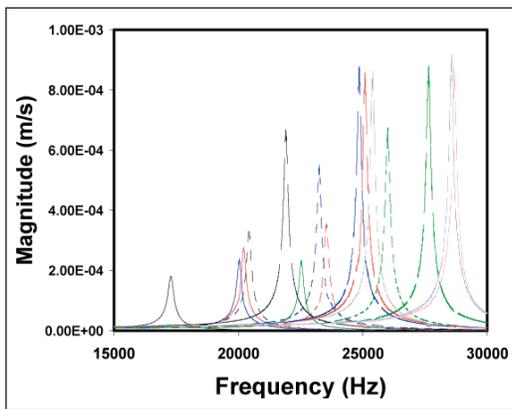


Figure 2. Resonant frequency response of micromachined CMOS cantilever test structures.

The method is based on the fact that the resonant frequency of the cantilevers is related to their elastic modulus, density, and the geometry. They can be fabricated with different combinations of layers and then comparisons of the resonant frequency can be used to extract the modulus of the individual layer. The cantilever test structures can be fabricated simultaneously with the fixed-fixed beams and measurements of residual strain

and strain gradient can be made. With the residual strains, from the fixed-fixed beam method, the elastic constant, from the resonant method, and the strain gradient, from the curvature of cantilevers, the residual stress and its gradient can be calculated.

DELIVERABLES: Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens.

ACCOMPLISHMENTS

Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; results for the same property by different measurement methods; and experimental results versus numerical simulations. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results. Currently we are placing major focus on the comparison of stress-to-failure a.c. electrical tests vs. microtensile tests. Figure 3 shows the effect of line width on current density at failure in ramp-to-failure tests.

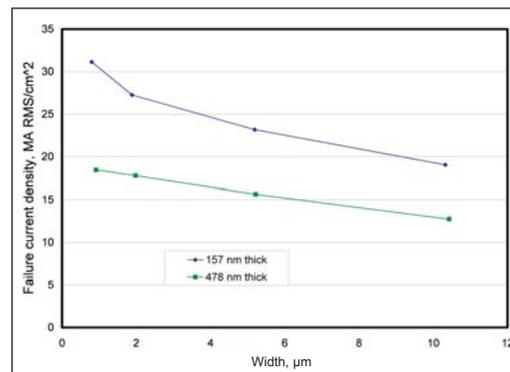


Figure 3. Effect of line width on current density at failure in ramp-to-failure tests in PVD copper films.

Such scale-related effects will have to be factored into analysis procedures for deducing material properties from a.c. tests. We are also running an interlaboratory round robin on the use of nanoindentation to measure hardness and modulus in a copper film on a silicon wafer. Specimens have been fabricated, characterized, and distributed to over 20 laboratories.

DELIVERABLES: Four technical presentations on the comparison of electrical and mechanical stress effects have been presented at technical conferences, 2Q 2004 to 2Q 2005, and three were submitted for publication in the respective technical conference proceedings. Three journal papers appeared in the past year. See Recent Publications, below.

A key experimental tool for understanding the sources of mechanical weakness is fractography of broken specimens. A new scanning electron microscope, with a field-emission source and an in-lens detector, is allowing us to obtain very clear images of the fracture surfaces of microtensile specimens. This aluminum CMOS contact metal had low elongation, and variable tensile strength with some very low values. We have made progress in mounting tested tensile specimens on silicon-nitride membranes for observation in the TEM. An image of a failed specimen is shown in Fig. 4.

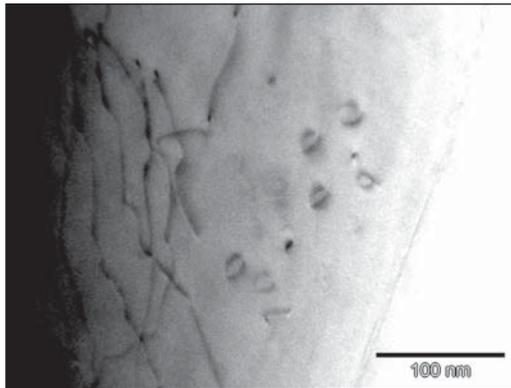


Figure 4. TEM image of failed edge of a MOSIS thin film aluminum tensile specimen, showing prismatic dislocation loops, but no mobile dislocations, in the region near the edge.

Recently, we have been working to demonstrate the applicability of these techniques to materials recently introduced in the microelectronics industry, specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5. We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 μm to 10 μm , increases the ductility from around 1 % or less to 5 % or more. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 $^{\circ}\text{C}$. Figure 6 shows recent results for contact Al-Si, from MOSIS, and electrodeposited copper, made at NIST.

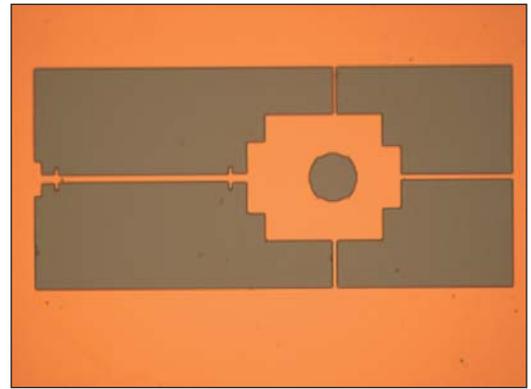


Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 μm wide by about 200 μm long.

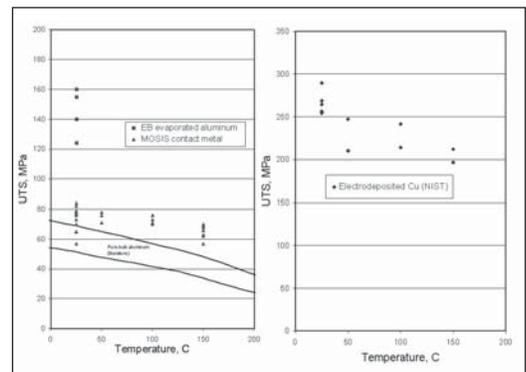


Figure 6. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

Figure 7a shows a high-resolution SEM image of the surface of an electrodeposited (ED) copper specimen made at NIST. The distinctive morphology, an array of joined spheres, may not be representative of normal production material. But it may represent, in an exaggerated form, microstructural features commonly present in ED copper. Its crystallographic symmetry, lattice parameter, and mechanical properties all appeared normal when measured by standard techniques. Figure 7b shows an atomistic model that simulates the mechanical behavior of this morphology, though at a smaller scale. The at-

oms shows as solid black are in regions of low face-centered-cubic symmetry, while the atoms shown in color are surrounded by near-perfect fcc structure. This simulation presents a possible explanation for our measured values of the elastic constant of ED copper, which are lower than the bulk value. We have extended our atomistic modeling to the mechanical behavior of quantum dot structures such as germanium in silicon and indium arsenide in gallium arsenide, specifically, the strain in and around the heterogeneous inclusion. Strains surrounding the quantum dot structures play an important role in creating the confined electron states and in providing a driving force for self-assembly of arrays of dots.

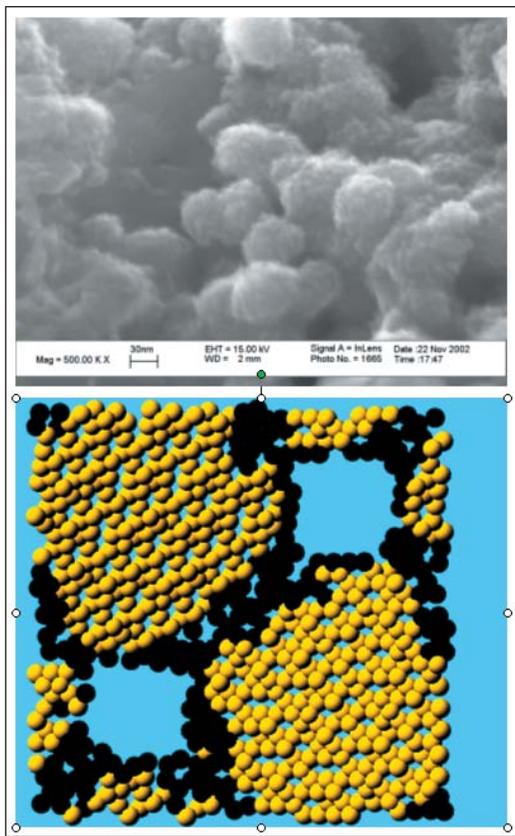


Figure 7. a) High-resolution SEM image of electrodeposited copper specimen made at NIST. The original magnification was 500,000. The copper “balls” are 30–50 nm in diameter. b) Atomistic model simulating the morphology and mechanical behavior of this copper electrodeposit. The atoms shown as copper-colored have near-normal face-centered-cubic crystal environments; the atoms shown as black are also copper atoms, but their local crystallographic symmetry is lower. Through the use of periodic boundary conditions, this 23000-atom model simulates a specimen of indefinite size.

Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. Figure 8 shows the large difference in lifetime seen under the AC and DC test conditions. We have pursued crystallographic mapping experiments within a field emission SEM, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 9, pg. 108). Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect.

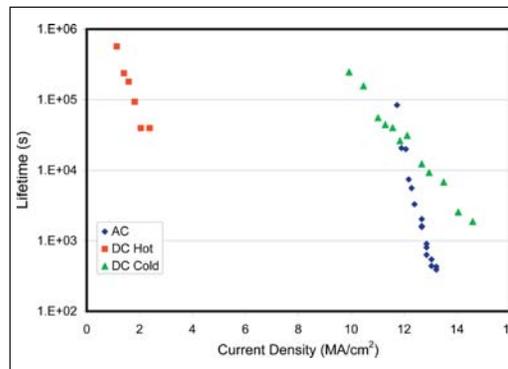


Figure 8. Time to open circuit under various electrical testing conditions. “AC” and “DC Cold” data obtained with specimen nominally at room temperature. “DC Hot” tested at nominal specimen temperature of 227 °C. “DC Hot” data from U. E. Möckl, M. Bauer, O. Kraft, J. E. Sanchez, Jr., and E. Artz, *MRS Symp. Proc.* Vol. 338, 373 (1994).

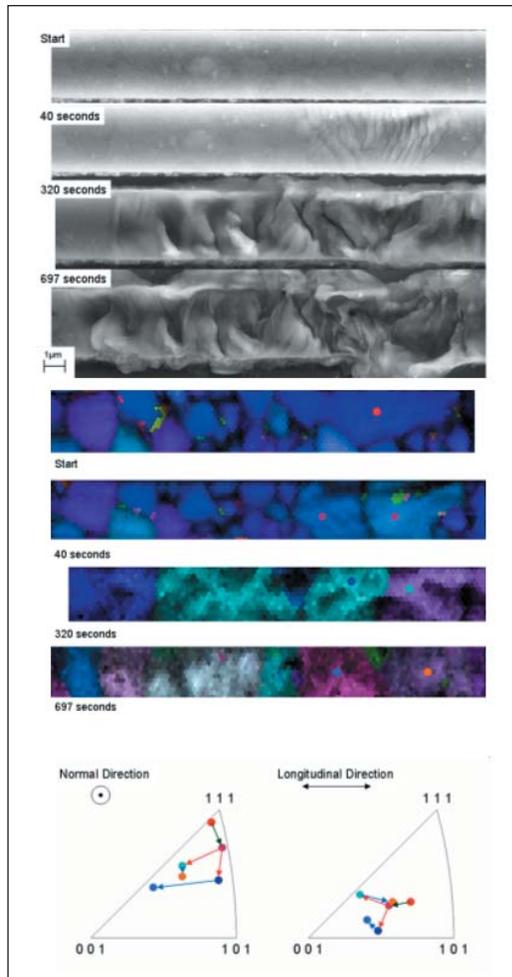


Figure 9. AC testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at 0, 40, 320, and 697 seconds of AC cycling at about 12 MA/cm². Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

Because it is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. A model has been developed for a composite cantilever beam. Preliminary measurements indicate that this technique can provide accurate values of the different layers in the interconnect structure, as well as insight into the behavior of the structure as a whole.

The Matlab optimization procedure to extract the Young's modulus values of the various interconnect and oxide layers has been automated. This procedure includes the calculation of the thicknesses of the various layers given inputs such as capacitances, sheet resistances, resistivities, and step height measurements.

Also, a sensitivity analysis has been semi-automated where each of the Matlab inputs gets varied $\pm 10\%$ or ± 3 standard deviations. The resulting Young's modulus values are then recorded. The important conclusion is that even if the various inputs are off by $\pm 10\%$, reasonable Young's modulus values can still be obtained. The optimization technique is not as sensitive to layer thicknesses as originally believed. The technique is proving to be solid and reliable.

The latest test chip design (see Fig. 10) includes cantilevers ranging in length from 100 μm to 400 μm . A procedure was developed using the optical vibrometer to obtain the resonant frequencies of the shorter length cantilevers. Plots of Young's modulus versus length for each layer exhibit phenomenal results. *The optimized Young's modulus results are stable as a function of length and within the realm of acceptability!* Figure 10 shows these plots for metal1 and metal2. The data points given at $L=500\ \mu\text{m}$ represent the averages from two previous chip submissions. The error bars on the data points represent a plus or minus one sigma variation. The minimum and maximum bounds represent values given in the literature. The line represented by 'Eguess' is the initial value used in the optimization. An ini-

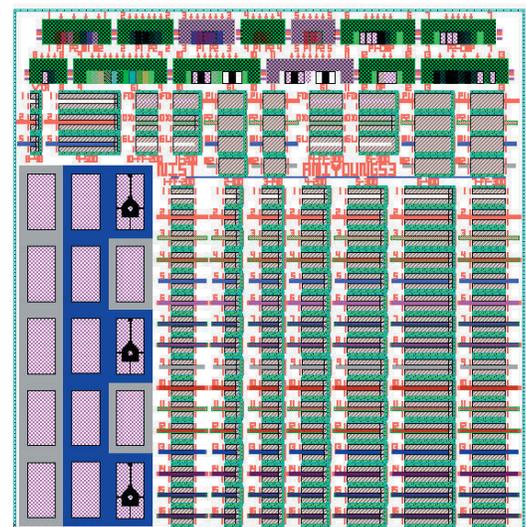


Figure 10. Test chip design fabricated on the AMI 1.5 μm CMOS process.

tial result from the tensile tests found an average metal1 and metal2 Young's modulus value of 63 GPa, which falls nicely between the metal1 and metal2 lines in Fig. 11. Journal articles are being prepared on both the Young's modulus results and the thickness results.

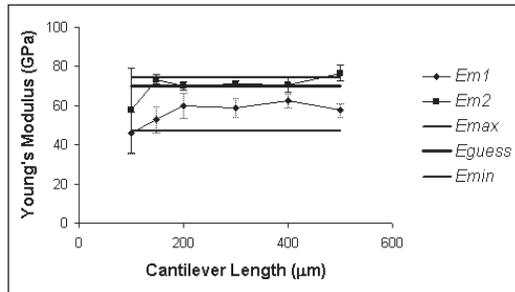


Figure 11. Young's modulus plotted versus cantilever length for metal1 and metal2.

COLLABORATIONS

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Motorola, Inc., AISL, Tempe, AZ, Betty Yeung, and MATC, Schaumburg, IL, Dr. Andrew Skipor

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. Tom Veriner.

RECENT PUBLICATIONS

R.R. Keller, and D.T. Read, "The NIST Workshop on Reliability Issues in Nanomaterials, August 17-19, 2004," Proceedings, Government Microcircuit Applications & Critical Technology Conference 2005, Las Vegas, NV, April 4-7, 2005.

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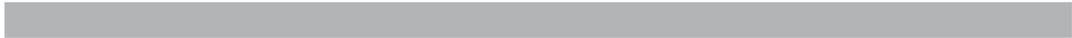
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INTERCONNECT TEST STRUCTURES

GOALS

The overall goal is to make essential contributions to a test-structure infrastructure that is responsive to state-of-the-art interconnect-system fabrication needs. Test-structure metrology applications can be classified into two groups: 1) selection of materials for developing fabrication processes for new interconnect systems that comply with always-increasing device density needs and maintaining those processes in wafer production 2) parameter extraction for modeling and predicting the performance of interconnect systems for particular fabrication implementations. The project's test structures for process development will allow the extraction, by electrical means, of key dimensional parameters such as etched-feature CD. This is a key unsolved problem when copper conductors are embedded in barrier metals. In this case, an as-yet unresolved issue is the adverse interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features. A near-term goal in related materials studies is the fabrication of electrically testable, all copper, features having lateral dimensions in the 20- to 100-nm range. This project's unique approach assesses the impact of feature-dimension scaling on the fundamental physics of electron transport in features built from single metal species, such as copper, without the metrology complications resulting from having other metal species incorporated into interconnect features. The information so provided is to enable modeling the performance of features that are replicated with two or more metals and is designed to aid in the verification of dimensional parameter extraction for process-control purposes. Another class of test structures for process maintenance, where the need for innovation is driven by scaling, is overlay standards. Among the test structures that will be implemented for modeling the performance of particular fabrication implementations will be strip lines that will be rf-tested from DC to 10 GHz, consistent with clock speeds of road-map integrated circuits over the next several years.

A related facet of this work is the measurement of the sheet resistance of planar films of preferred interconnect metals, such as copper, having thicknesses in the 20-to-100 nm range. The purpose is to relate electrical performance to material properties such grain-size distribution and the films' thicknesses. It is anticipated that this ap-

proach will make major contributions to the correct interpretation of the electrical measurements of the narrow features described above.

CUSTOMER NEEDS

Interconnect is becoming the principal factor that determines the maximum performance that can be attained with emerging generations of gigascale chips. This means that future advances in IC performance will be governed increasingly by the advances in interconnect technology, rather than by advances in active devices. In particular, at technology nodes of 0.13 μm and below, the attainable rate of signal propagation through the IC chip is dominated by the interconnect implementation. As aluminum is replaced by hybrid copper/barrier-metal conductors, the initial benefits of the higher conductivity, which are real at the 130-nm node, are becoming problematic at the 90-nm node and below, as a result of the predominance of contributions of the barrier metal to the conductor resistance. Whereas there is no simple global solution to the challenge at this time, it is certain that advances in metrology science applied to process and materials management, such as those being pursued by this project, will play a central role in assuring maximum performance from copper-based interconnection systems until such time that innovations, such as optical interconnects, are introduced. Meanwhile, a manufacturing challenge that is as attributable scaling *per se* rather than the materials selected for interconnect implementation is overlay. Overlay metrology is being challenged by exacerbation of the tool- and wafer-induced shifts that are generally manageable for technology generations introduced prior to the 130-nm node.

TECHNICAL STRATEGY

The four-part current technical strategy is to build on opportunities afforded by the project's unique SCCDRM experience. The same substrates that have been developed for CD reference-material applications are being applied to the fabrication of single-metal, initially copper-only, test structures with features having lateral dimensions in the 20- to 100-nm range. The process-flow is illustrated in Fig 1 (pg. 112). The approach shown there will provide a definitive assessment of the impact of feature-dimension scaling on the fundamental physics of electron transport in narrow features patterned from copper, without the resistance

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metrology complications resulting from having other metal species serve as barrier layers. The information so provided will enable modeling the performance of features that are replicated with copper-cored binary-metal technology and will aid in the verification of dimensional parameter extraction for process-control purposes.

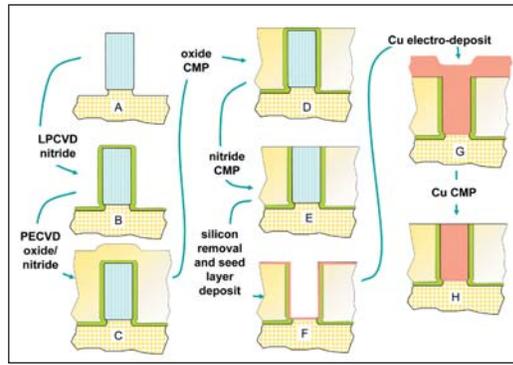


Figure 1. Scheme for fabrication of single-metal, test structures with features having lateral dimensions in the 20-to-100 nm range.

The project's test structure is one that will allow the extraction, by electrical means, of key dimensional parameters for process-control purposes such as copper-cored interconnect feature CD. This responds to an unsolved problem when copper conductors are embedded in barrier metals. The solution is sought after by companies marketing interconnect-system modeling software tools and their industry clients. Our strategy is based on a test structure we first proposed four years ago but have not yet been implemented.

To validate CD and interconnect feature resistance extraction from test structures, we are initiating a study of the interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features. There is an absence in the scientific literature of any report of analyses of this central issue.

Another class of test structures for process maintenance, where the need for innovation is driven by scaling, is overlay standards. This project has successfully filed for a patent on an electrically calibrated test structure to serve as a process- and tool-specific overlay standard that avoids all the limitations of other approaches.

Among the test structures that are being designed for modeling-parameter extraction are strip lines that will be rf-tested from DC to 10 GHz, consistent with clock speeds of road-map integrated

circuits over the next several years. The strategy is the computation of rf-impedance properties that are employed in interconnect-system modeling from S-parameter measurements. An important spin-off from this activity is the application of similar rf-measurement techniques to traceably validating key dimensional parameters of masks which are patterned for interconnect fabrication, another application which has been long sought by the mask-vendor and mask-user industries. This work will be done initially on binary masks but, if successful, will be extended to the examination of opportunities in dimensional metrology for more complex binary-mask applications.

A related facet of this work is the measurement of the sheet resistance of planar films of preferred interconnect metals, such as copper, having thicknesses in the 20- to 100-nm range. The purpose is to relate electrical performance to material properties such grain-size distribution and the films' thicknesses. It is anticipated that this approach will make major contributions to the correct interpretation of the electrical measurements of the narrow features described above.

DELIVERABLES: Complete an analysis of the effects of surface and grain-boundary scattering that characterize dc conduction through planar films. 3Q 2005

DELIVERABLES: Design, and verify by simulation, the performance of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication. 3Q 2005

DELIVERABLES: Design, fabricate with SCCDRM technology, and make initial ECD measurements on a test chip having chemically stable copper-only features. 4Q 2005

DELIVERABLES: Design, fabricate, and make initial ECD measurements a second-generation SCCDRM test chip having chemically stable copper-only features and perform silicon-feature silicidation process. 4Q 2005

DELIVERABLES: Design an interconnect test chip for extracting s-parameters and rf-impedance components over frequency ranges up to 20GHz. 1Q 2006

DELIVERABLES: Fabricate, test, and calibrate a selection of overlay test chips designed for high-density interconnect applications. 2Q 2006

DELIVERABLES: Fabricate a strip-line interconnect test chip for s-parameter extraction, and measure rf-impedance components over frequency ranges up to 20GHz interconnect-modeling applications. 3Q 2006

ACCOMPLISHMENTS

Since this project has only been at full strength for several months, the major accomplishments are largely of a preparatory and logistical nature. However, several important ones have been attained.

- *The first draft of a paper on effects of surface and grain-boundary scattering that characterize dc conduction through thin planar films has been completed.* The thrust of this work is to provide essential input for modeling conductor resistance as influenced by electron scattering by the conductor's surfaces and grain boundaries, and the effects of barrier layers on copper line resistance.

- **Standards Leadership:** Project member served on JEDEC Committee JC14.2 to update one existing JEDEC standard and complete a new JEDEC standard.

Both of these standards deal with interconnect reliability. The existing standard, JEP139, is for characterizing the resistance of interconnects to stress voiding damage and previously only applied to aluminum interconnect. JEP139 is being modified to include applicability to copper interconnects and has completed two rounds of balloting. The new standard will also deal with copper interconnects, and is a test standard for electromigration and is in the process of undergoing first ballot.

- *The CAD of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication has been completed.* A program to simulate and validate the calibration of the standard is nearing completion.

- *The fabrication with SCCDRM technology of the first test structures having chemically stable, copper-only, features has completed copper seed-layer deposition and the first wafers are being electro-plated.* The approach shown there will provide a definitive assessment of the impact of feature-dimension scaling on the fundamental physics of electron transport in narrow features patterned from copper, without the resistance metrology complications resulting from having other metal species serve as barrier layers.

- *The CAD of a second-generation SCCDRM test chip for the fabrication chemically stable copper-only features has entered planning stages.*

The principal goal is to reduce the CDs we are presently fabricating with i-line lithography to the 20- to 40-nm level with the use of Imprint and direct-write e-beam lithography. These are the features that will eventually be used for silicidation experiments. The collaborating partner has already been supplied project test chips having silicon features with 50-nm CDs for familiarity and preliminary process tests.

- *The project competed for, and was awarded, an intra-mural program to conduct further research into SCCDRM fabrication and calibration.* This program is providing major infra-structure benefits in the meeting the deliverable item schedule above/.

COLLABORATIONS

The leading collaborators are three Universities.

The Scottish Microelectronics Centre at the University of Edinburgh (SMC) is now providing almost all wafer the project's wafer fabrication operations. More importantly, the staff there are highly and broadly experienced in interconnect fabrication materials, processes, and issues. Audio teleconferences are exchanged between Project and SMC staff at least once a week. Its wafer-fabrication facility is very well equipped to meet many of the project's needs and will continue doing so for the foreseeable future with government funding. Its receiving the latter was an early product of our collaboration.

The Electrical-Engineering and Computer-Sciences Department at George Washington University has been funding the studies of Ph.D students, and a Professor, to work on this NIST Project for almost a decade. The present collaboration contributes special skills in rf parameter extraction and the physics of electron transport.

A new collaboration with the **Department at The University of Texas at Austin** is in the formative stages. UT-Austin's role will be to conduct experiments on the transformation of narrow SCCDRM features to silicide material and to contribute very desirable ultra-narrow-line lithography for the next-generation SCCDRM fabrication.

The project has collaborated over the past several years with personnel at **Cadence Systems, Inc.** The collaboration initially involved in refining ECD test-structure metrology to address the binary-metal conductor problem described earlier in this document. More recently, the collaboration attention has been shifted to parameter extraction

from rf test structures for modeling interconnect-system performance of 90-nm generation devices.

Important collaborations with **two different major semiconductor-industry players** are in the formative stages. The respective and separate topic fields are electrically-calibratable overlay standards and non-contact CD metrology for interconnect features. The two companies are not identified here because both sets of CRADA negotiations are in a sensitive stage.

This project has always benefited from very active collaboration with Litho-Metrology Operations at **SEMATECH**. Although the project's focus has only recently shifted away from litho-metrology to interconnect, we are actively pursuing a parallel shift in our collaboration.

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WIRE BONDING TO COPPER/LOW- κ SEMICONDUCTOR DEVICES

GOALS

The overall objective is to determine optimal conditions for achieving high yield reliable fine-pitch wire bonds to advanced technology semiconductor chips with copper/low- κ interconnect structures.

CUSTOMER NEEDS

The introduction of copper metallization interconnect structures in advanced integrated circuit manufacture has forced changes in wire bonding. The process should be invisible to the current wire bonding machines. However, bare-copper bond pads oxidize, requiring an oxygen-protective/bondable coating. The current solution of using a tantalum barrier, capped with aluminum, for bondability is unsatisfactory for fine pitch due to increased Au-Al intermetallic failures. Also, when low-modulus low-dielectric materials lie below the pad, a support structure is necessary to prevent damage to the interconnection/dielectric layers. There are many approaches to solving these various problems; the NIST program is attempting to optimize and develop new bond pad solutions where necessary (Fig. 1).

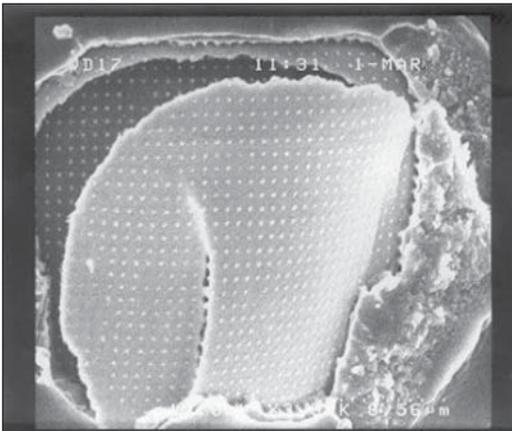


Figure 1. Pad peeling is a common problem with Low- κ under the bond pad.

TECHNICAL STRATEGY

1. The industry is generally using a tantalum barrier with an aluminum cap for wire bonding. Such an approach requires several expensive (deposition, mask, etch, clean) wafer preparation steps. It also suffers from serious intermetallic failure problems as the pad pitch is reduced be-

low 50 μm . A better approach to protecting the copper is to coat the bond pads with a bondable gold layer. This is more direct and eliminates the intermetallic problem in the process. For this approach, the first objective is to determine the diffusion coefficients of copper through gold, because copper can diffuse to the surface during thermal processes, and will oxidize, preventing good bond formation. Literature values on various gold platings are contradicting and have been performed on non-damascene structures, often with undefined plating conditions. A more classical approach, but also a more difficult process, using SIMS has been proposed. We have developed several gold deposition process over the damascene process copper metallization chips. Even without the actual diffusion coefficients, a pragmatic approach is being carried out by heating gold coated samples (with various grain refiners) and doing extensive wire bonding and evaluating with ball shear tests. A subset of this work will be to determine the minimum thickness of gold necessary to prevent copper diffusion/oxidation in normal bonding/processing temperatures. Several inorganic coatings for protection have been evaluated. Sandia has applied thin deposited SiO_2 coatings on copper wafers and they were evaluated. Results indicated that all coatings were nonuniform, but bonding did occur on the better pads. This evaluation is continuing, but preparing uniform coating that are thin enough to bond through has proven difficult (Fig. 2, pg. 116).

2. Another objective is to measure the nano-hardness and modulus of the damascene copper in order to optimize bonding, [hardness should be minimized (80 Knoop to 100 Knoop)]. This was successful, and results indicate that annealing in argon produce the softest most bondable copper surface for bonding.

Problems occurred when sawing the bare copper chips in which the saw particles stick to the bare copper. Several approaches to curing this problem were pursued and one has been adopted. (Wafers are sawed face down on tape within $\sim 10 \mu\text{m}$ of completion. They are snapped off upon removal from the tape, resulting in clean chips. Copper damascene process samples have been supplied by IBM and SEMATECH for this effort.

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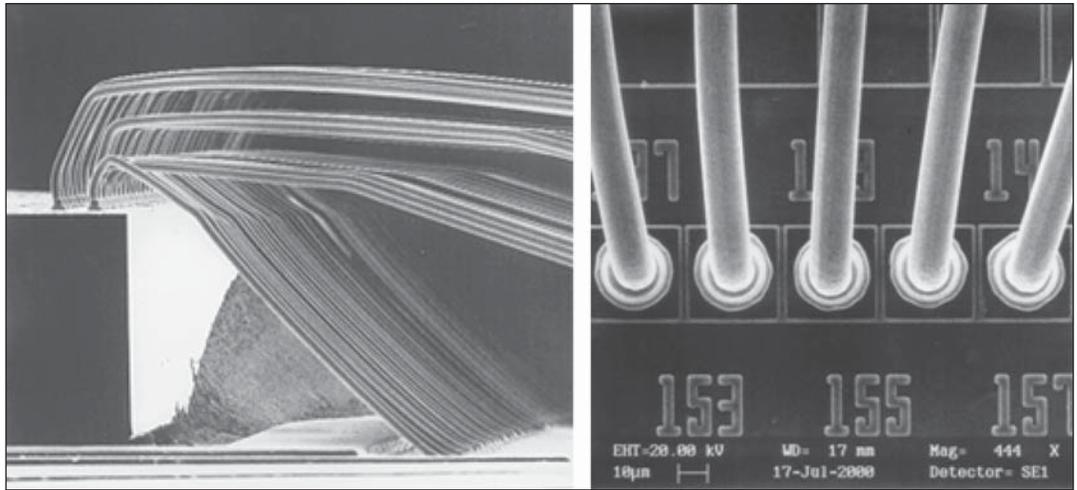


Figure 2. Area Array wire bonds at 35 μ pitch (ASM bonder)

DELIVERABLES: The desired thickness of gold deposition will be determined, as well as the most desirable grain refiners for the purposes. A nickel strike coating also was developed. Two different plating additives are being evaluated. Diffusion studies of copper into gold will be made after evaluating the surface morphology. The applicability to fine pitch bonding to the gold surfaces will be evaluated. 3Q 2005

satisfactory and bonded well. Currently, wafers from another source with thicker copper are being plated. Copper diffusion through the gold is being measured.

ACCOMPLISHMENTS

- Knoop hardness measurements have been accomplished with a series of annealing experiments made with copper chips, and pragmatically verified by actual bonding experiments. Values of measured nanohardness have been dependant on the annealing gas (argon is best) and have been as low as 60 GPa (about 120 GPa unannealed) and the modulus as low as 20 GPa. Problems have occurred in early diffusion studies and several different methods are being initiated.

- Papers published, entitled “Wire Bonding To Advanced Copper-Low- κ Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations,” by George G. Harman and Christian E. Johnson, Proc. 2001 IMAPS Symposium, Oct 9-11, 2001, Baltimore, MD, pp. 484-491. This paper won an award as an outstanding paper in the Symposium. An updated version, with new data, was published in the IEEE Transactions on Components and Packaging Technologies, V-25, Number 4, Dec. 2002, pp. 677-683. A talk sponsored by the IEEE CPMT society was given in San Jose in May 2003.

- The two step non-contact gold deposition process used on some of the original SEMATECH wafer copper etched the copper surface, whereas other gold deposition methods were

SOLDERS AND SOLDERABILITY MEASUREMENTS FOR MICROELECTRONICS

GOALS

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions, the broadening use of flip-chip technology, and the movement toward environmentally friendly lead-free (Pb-free) solders. To support needs in this area, the goal of this project is to provide data and materials measurements of critical importance to solder interconnect technology for microelectronics assembly.

CUSTOMER NEEDS

The U.S. microelectronics industry has clearly articulated measurement needs for solderability and assembly, especially for Pb-free solders. For example, the urgency for materials data for Pb-free solders has been specified in the 2002 iNEMI, 2003 IPC, and 2003 ITRS Roadmaps. The European Community (EC) directives on Waste Electrical and Electronic Equipment (WEEE) and the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) take effect in mid 2006. U.S. manufacturers must comply with these requirements in order to compete in the global market. These industrial needs are addressed under this NIST project.

Additional needs have been identified through participation in the International Electronics Manufacturing Initiative (iNEMI) working group on Pb-free solder alloys. It was learned that significant industrial problems had arisen due to contamination of Pb-free solders by the Pb contained in the protective solder coatings that are used on copper (Cu) leads. The protective layer deposited on Cu is usually referred to as a "pretinned" coating and is required to maintain solderability of the component during storage prior to assembly. Pb-free coatings of nearly pure tin (Sn) tend to grow "whiskers," however, which can cause shorts across leads. Thus the development of Pb-free alloy platings to replace Pb-containing protective layers is considered important, and tests which ascertain the tendency to form whiskers are much needed. NIST co-chairs the iNEMI Sn Whisker Modeling Group and is an active participant in the iNEMI Accelerated Sn Whisker Test Group.

TECHNICAL STRATEGY

We are providing the microelectronics industry with measurement tools and data to address solder interconnect problems. For example, a thermodynamic database has been developed and publicly distributed for modeling the processing behavior of lead-free solder systems. These databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will continue to be expanded and distributed via the web. We also provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations. In addition, a much-needed guide to interpretation of thermal analysis data will be produced.

It is well known that the use of pure Sn protective deposits has serious problems. Sn whiskers (filamentary whiskers typically 1 μm diameter and several mm long) can grow from the plating and cause electrical shorts and failure. Historically Pb was added to Sn plate to prevent whisker growth as well as to lower cost. In the current research program, it was decided to focus on Pb-free Sn-rich deposits with alloying additions that might retard whisker formation. The Sn-Cu system was selected for compatibility reasons, since Sn-Cu-Ag is likely to be the Pb-free solder of choice for industrial application. The substitution of a different solute for Pb in the Sn-rich deposit was proposed to also retard whisker growth. A detailed microstructural comparison of deposits with high and low whiskering tendency has been conducted. Sn grain size, shape, and residual stress have been measured and correlated to whisker growth (Fig. 1, pg. 118).

DELIVERABLES: Add pages for constituent binary and ternary phase diagrams containing Antimony to the Metallurgy Division Web book. 4Q 2005

DELIVERABLES: Make the easy-to-use lever rule equilibrium and Scheil solidification interface for solder solidification available on the web; make more complex thermodynamic programs available for download. 4Q 2005

DELIVERABLES: Finish Best Practice Guide for Differential Thermal Analysis. 4Q 2005

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Maureen Williams

"I consider your [NIST Metallurgy Division] group a key asset to industry in making these decisions on the soundest possible scientific basis. There is no comparable body of expertise anywhere in the world that matches that found in your group."

*Dr. George T. Galyon (IBM)
-Chairman, NEMI Tin Whisker
Modeling Committee*

DELIVERABLES: Electrodeposit Sn and Sn-Cu on W and Zn substrates to determine whisker tendency. Sn does not form intermetallic with these substrates. 4Q 2005

ACCOMPLISHMENTS

- 1) An easy-to-use lever rule equilibrium and Scheil solidification GUI interface has been prepared for solder solidification calculations. The code allows the user to select the default NIST thermodynamic data base or a user defined data base. The user selects a composition in either weight or atomic percent and chooses an equilibrium or Scheil calculation. Results are presented in either graphical or tabular form showing the starting temperature of solidification and the final freezing temperature as well as the phase that occur as eutectic microconstituents.
- 2) NIST remains a co-chair in the iNEMI Sn Whisker Modeling Group (working closely with members ChipPAC, Cookson, Delphi Delco, FCI Framatome, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas

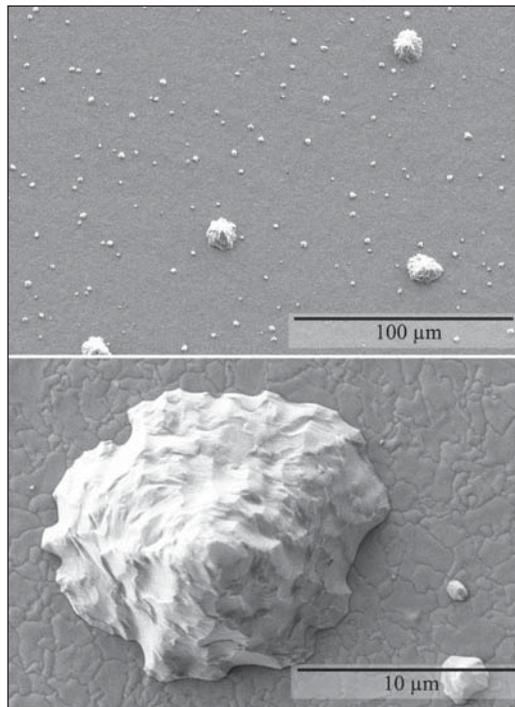


Figure 1. Low and high magnification SEM micrographs of the electrodeposit surface of a 16 μm thick pure Sn electrodeposit on a cantilever beam showing bimodal size distribution of conical hillocks. Such hillocks form to relieve compressive residual stress. Whiskers form when grain boundaries in the deposit are pinned by precipitates.

Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics) and is an active participant in the iNEMI Accelerated Sn Whisker Test Group.

- 3) JEDEC Solid State Technology Association (formerly known as the Joint Electron Device Engineering Council), excepted and published the iNEMI test protocol “Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes” as JEDEC Standard JESD22A121 in May 2005. NIST researchers provided input for this protocol.
- 4) A major accomplishment of this year is the submission of a manuscript to *Acta Materialia* entitled, “Hillock and Whisker Formation in Sn, Sn-Cu and Sn-Pb Electrodeposits.” The paper presents measurements of compressive stress in the electrodeposits and how the different microstructure of the deposits effect whisker growth. Relief of the compressive stress occurs by uniform creep for Sn-Pb because it has an equiaxed grain structure. Localized creep in the form of hillocks and whiskers occurs for Sn and Sn-Cu because both have columnar structures. Compact hillocks form for the Sn deposits because the columnar grain boundaries are mobile. Contorted hillocks and whiskers form for the Sn-Cu deposits because the columnar grain boundary motion is pinned by intermetallic precipitates.

- 5) Some reports suggest that restraining and cracking of the Sn oxide surface film are necessary steps in the nucleation of Sn whiskers. However, results at NIST, accepted for publication in the *Journal of Electronic Materials*, showed little support for this mechanism. For instance, we observed whiskers only on bright Sn-Cu electrodeposits but not on pure bright Sn electrodeposits on pyrophosphate Cu substrates. Thus, in order to understand the role of the deposit surface, the Sn oxide surface film and surface structures were analyzed by Auger and EBSD. Especially, in Auger analysis, residuals of the Sn oxide surface film were observed after Ar^+ ion cleaning. This feature allowed us to discriminate the Sn whisker growth with or without the oxide surface film. In EBSD analysis, grain and eruption orientations of the Sn deposit were characterized, and the results were discussed in metallurgical terms in order to correspond to the Sn whisker growth.

COLLABORATIONS

International Electronics Manufacturing Initiative; Lead-free Solders and Reliability. Co-Chair of the Sn Whisker Modeling Group and a member of the Accelerated Sn Whisker Test Group.

RECENT PUBLICATIONS

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