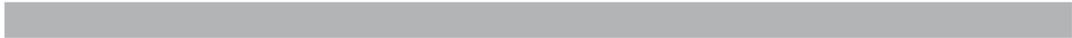


## **DEVICE DESIGN AND CHARACTERIZATION PROGRAM**

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as FINFETs, fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube and molectronic device structures need to be characterized. Another addition to the portfolio is the emerging field of organic materials electronics. To this end we have initiated a new program, “Device Design and Characterization.” One project that has to be highlighted because it will impact all the projects in the portfolio over time is the Advanced Measurements Nanofabrication Facility Support project. With the completion of the Advanced Measurements Laboratory on the Gaithersburg, Maryland campus, we have begun to populate a cleanroom facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.



# DEVICE CHARACTERIZATION AND RELIABILITY

## GOALS

The goal of the Advanced Device Characterization and Reliability Project is to improve and develop reliability and electrical characterization tools for advanced CMOS technologies. Deliverables include test methods, diagnostic procedures, reliability data, electrical characterization methods, physical models for wear-out, and methodologies to determine energy band diagrams for metal/high- $\kappa$  systems.

A specific focus is to increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (*i.e.*, the gate dielectric, SiO<sub>2</sub>, and the gate electrode, doped polycrystalline Si), which has served the industry for 35 years, must now be entirely replaced with one having a higher capacitance and lower power dissipation. Gate dielectrics having higher dielectric constants than SiO<sub>2</sub> will replace SiO<sub>2</sub>, and metal electrodes will replace polycrystalline silicon. The enormous complexity of selecting the proper combinations of new gate dielectrics and gate metal electrodes can only be attacked using combinatorial materials methodologies. Therefore, we will be implementing this technology.

## CUSTOMER NEEDS

The MOSFET (Metal Oxide Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 2 nm is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) with effective thickness values of 1.4 nm, or less, being projected in 2004, dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below  $\sim 2.0$  nm, SiO<sub>2</sub> must be replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal-silicates or metal silicates.

Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO<sub>2</sub> of this thickness, a high permittivity gate dielectric (*e.g.*, Si<sub>3</sub>N<sub>4</sub>, HfSi<sub>x</sub>O<sub>y</sub>, ZrO<sub>2</sub>) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO<sub>2</sub> and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO<sub>2</sub>, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

## TECHNICAL STRATEGY

There are two main focus areas for this project:

- Developing electrical and reliability characterization techniques for ultra-thin SiO<sub>2</sub> and high dielectric constant gate dielectrics.
- Develop combinatorial (fast, local) measurement techniques to measure appropriate electrical properties on gate stacks consisting of new gate dielectric and gate metal electrode materials.

The first focus area is to develop robust electrical characterization techniques and methodologies to characterize charge trapping kinetics, threshold voltage  $V_t$  instability, defect generation rates and time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of

## Technical Contacts:

John Suehle  
Eric Vogel  
Martin Green

the characterization schemes will first be developed on the simpler ultra-thin oxide and oxidenitride dielectrics and then be applied to the metal oxide and silicate dielectrics for a variety of high- $\kappa$  samples subject to different deposition and gate electrode processes. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization.

**DELIVERABLES:** Study of Negative Bias Temperature Instability in  $\text{HfO}_2$  transistors under pulsed bias stress. 1Q 2005

**DELIVERABLES:** Perform CV test methodology for extracting metal/high- $\kappa$  work function from various high- $\kappa$  metal gate systems, 2Q 2005

**DELIVERABLES:** Provide test technique(s) and analysis to quantify electrical trap densities at multiple interface stacks by 3Q 2005.

**DELIVERABLES:** Compare metal work function measurements with measurements performed with other techniques including internal photo emission and scanning Kelvin probe microscopy on ternary metal systems produced by combinatorial techniques. 3Q 2005

**DELIVERABLES:** Identify suitable metal gate electrode compositions, based on barrier height and thermal stability criteria, for use with state-of-the-art gate dielectrics (e.g., Hf-Si-O-N). 4Q 2005

## ACCOMPLISHMENTS

### NEGATIVE BIAS TEMPERATURE INSTABILITY (NBTI) STUDIED FOR $\text{HfO}_2$ P-MOSFETS

The contribution of gate oxide bulk traps to NBTI degradation of  $\text{HfO}_2$  devices was evaluated and compared with  $\text{SiO}_2$  control samples. The  $\Delta V_{th}$  and oxide trap generation of  $\text{HfO}_2$  and  $\text{SiO}_2$  devices show a dependence on gate pulse repetition frequency as shown in Fig. 1. Besides interface traps, bulk traps also influence the NBTI degradation of  $\text{HfO}_2$ , and this influence is also dependent on the stress conditions. At dc stress conditions, the bulk trap generation is comparable to that of interface traps, and thus plays an important role for the  $\Delta V_{th}$ , however it becomes negligible at higher pulse repetition frequencies. In addition

to the different frequency response, the bulk trap generation also shows a different temperature dependence than the interface traps. We found that interface traps generation has much higher activation energy than bulk traps, which also explain the different temperature dependences of  $\Delta V_{th}$  at dc and high frequency stress conditions.

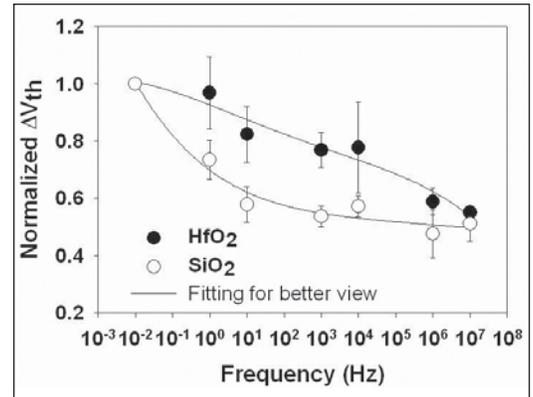


Figure 1. Plot comparing NBTI induced threshold voltage shift versus pulse repetition frequency for  $\text{SiO}_2$  and  $\text{HfO}_2$  films.

### MECHANISTIC STUDY OF PROGRESSIVE BREAKDOWN IN SMALL AREA ULTRA-THIN GATE OXIDES

A study was completed to investigate two competing post soft breakdown modes observed in ultra-thin gate oxides. One breakdown mode features a conducting filament that is stable until hard breakdown occurs and a second mode features a filament that continually degrades with time. Figure 2 shows an example of an unstable breakdown filament. The figure shows the current versus time characteristic for a 2 nm thick gate oxide sample. After dielectric breakdown, the current becomes noisy and eventually increases with time. The acceleration factors are different for each mode, indicating different physical mechanisms are involved in the evolution and formation of the final hard breakdown event. Unstable filaments that result from the first soft breakdown progressively degrade and change physical structure until their leakage current becomes unacceptably large. A set of voltage and temperature acceleration parameters different from oxide wear-out are necessary to project the leakage current with time.

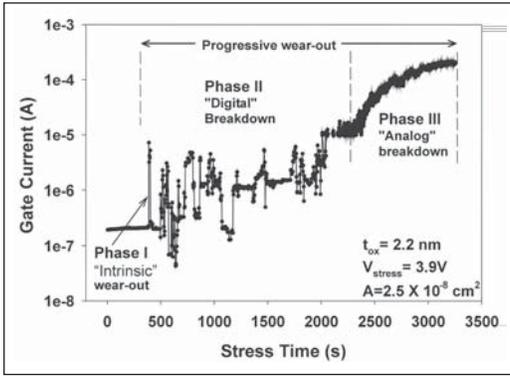


Figure 2. A typical current vs time characteristic for a 2 nm thick gate oxide that has experienced soft breakdown with the formation of non-stable conducting filament.

### COMBINATORIAL METHOD FOR STUDYING TERNARY METAL GATE SYSTEMS

Combinatorial methodologies were used to identify, from large candidate metal alloy systems, those alloys that possess the right combination of electrical properties and thermal stability required for metal gate electrodes. The C-V and I-V characteristics of hundreds of capacitors, each with a different metal gate alloy composition, were then automatically measured. A CV simulation program was then used to extract capacitor parameters. Figure 3 shows  $V_{fb}$  data, extracted from C-V plots using the simulation program, for Nb-Pt-W alloys deposited on a 6 nm  $HfO_2$  film. Note the distinct variations in  $V_{fb}$  that can be discerned as a function of composition in the ternary system.

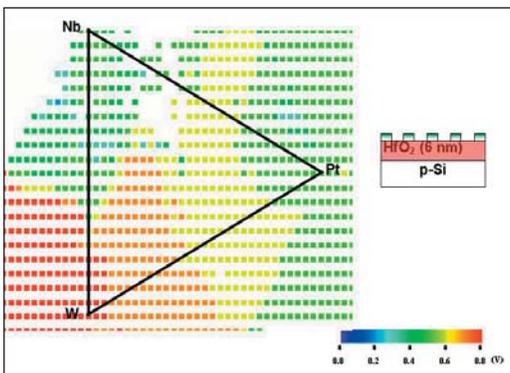


Figure 3. Two dimensional plot showing the variation of CV flatband voltage for a ternary metal system (Nb-Pt-W/ $HfO_2$ ) deposited by combinatorial techniques.

### MODIFIED CHARGE PUMPING TECHNIQUE TO EXTRACT SPATIAL DISTRIBUTIONS OF TRAPPING CENTERS IN $HfO_2/SiO_2$ STACKED DIELECTRICS

Analysis methodology for charge pumping (CP) data was developed and applied to extract the spatial depth profile of traps in the  $SiO_2/HfO_2$  gate stacks. This analysis indicates that by changing CP measurement parameters it is possible to probe traps at different depth inside the dielectric as shown in Fig. 4. Spatial profile of traps reveals three separate regions of trap location: in  $SiO_2$  interface,  $SiO_2/HfO_2$  interaction region, and an  $HfO_2$  film.

From the simulation result it has been shown that interface trap density during CP characterization is not equal to the total trap density in high- $\kappa$  gate stacks. It is also shown that the probable range of traps in the dielectrics is affected by the pulse parameters. These results are essentially important when experimental data from different electrical characterization techniques are compared. By using the proposed analysis, trap spatial profiles in the high- $\kappa$  gate stacks with different  $SiO_2$  interfacial layer thickness can be studied. The results clearly show the change of trap density from the  $SiO_2$  layer to the  $SiO_2/HfO_2$  interaction region and finally the  $HfO_2$  layer. Although an accurate depth position of traps cannot be determined due to unknown values of certain dielectric parameters, the relative shift of the trap depth profile is consistent with the difference of the interfacial layer thickness in different  $SiO_2/HfO_2$  stacks.

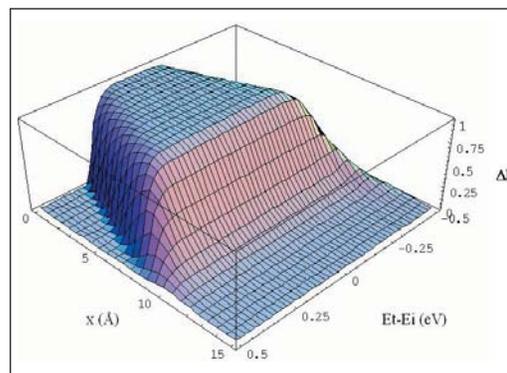


Figure 4. 3-D  $\Delta F$  contour simulation result.  $\Delta F$  is equal to one within the trapezoidal plateau that indicates the region having the maximum probability been probed.

## STANDARDS COMMITTEE PARTICIPATION

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

## COLLABORATIONS

IBM, Alternative Gate Dielectrics

N.C. State University (oxynitrides, nitrides, ultra-thin SiO<sub>2</sub>), alternative gate dielectrics

SEMATECH Characterization of metal gate high- $\kappa$  systems.

Sharp Microelectronics, Characterization of Hafnium-oxide dielectric films

Rutgers University, Characterization of high- $\kappa$  gate dielectrics

Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides

University of Maryland, College Park, ultrathin gate oxide reliability

U. Texas at Austin, Optical properties of ZrO<sub>2</sub> and HfO<sub>2</sub> for use as high- $\kappa$  gate dielectrics

## RECENT PUBLICATIONS

(Invited) J. S. Suehle, "Ultra-Thin Gate Oxide Breakdown: A Failure That We Can Live With," *Electronic Device Failure Analysis*, vol. 6, no. 1 (February 2004).

(Invited) J. S. Suehle, "Reliability Implications of Scaling Gate Oxides in Deep Submicron CMOS Technologies," 2004 GOMACTech, Monterey, CA, March 2004.

(Invited) J. S. Suehle, "Reliability Year In Review: Gate Dielectrics," 2004 IRPS

(Invited) Eric M. Vogel, "Characterization Needs for Emerging Research Materials and Devices," ITRS Emerging Research Materials Workshop, San Francisco, CA, July 11, 2004.

(Invited) E. M. Vogel, "Challenges of Electrical Measurements of Advanced Gate Dielectrics in MOS Devices," *Applied Materials*, Feb. 9, 2004.

(Invited) J. S. Suehle, "Reliability Challenges for Advanced Gate Dielectrics and Implications for Lifetime Projection," 2004 Microelectronics Reliability Qualification Workshop, Manhattan Beach, CA, Dec 2004.

(Invited) J. S. Suehle, B. Zhu, Y. Chen, and J. B. Bernstein, Detailed Study and projection of Hard Breakdown Evolution in Ultra-thin gate Oxides, *Microelectronics Reliability*, 45, p. 419 2005.

B. Zhu, J. S. Suehle, and J. B. Bernstein, "The Contribution of HfO<sub>2</sub> Bulk Oxide Traps to Dynamic NBTI in pMOSFETs," 2005 IRPS, San Jose, CA 2005.

B. Zhu, J. S. Suehle, and J. B. Bernstein, "Mechanism of Dynamic NBTI of pMOSFETs," Proceedings IEEE Integrated Reliability Workshop, Oct 18-21, 2004.

S. Sayan, T. Emge, E. Garfunkel, X. Zhao, L. Weilunski, R. A. Bartyński, D. Vandebilt, J. S. Suehle, S. Suzer, M. and Banaszak-Holl, "Band Alignment issues related to HfO<sub>2</sub>/SiO<sub>2</sub>/p-Si Gate Stacks," *J. Appl. Phys.* vol.96, No. 12, p. 7485 2004.

J.-P. Han, S. M. Koo, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, J. S. Suehle, "Reverse Short Channel Effects in High- $\kappa$  Gated nMOSFETs," 13th Workshop on Dielectrics in Microelectronics, Kinsale, Ireland, June 28, 2004.

J. S. Suehle, B. Zhu, Y. Chen, and J. B. Bernstein, "Acceleration Factors and Mechanistic Study of Progressive Breakdown in Small Area Ultra-Thin Gate Oxides," 2004 IRPS, Phoenix AZ, 2004.

B. Zhu, J. S. Suehle, and J. B. Bernstein, "Mechanism for Reduced NBTI Effect Under Pulsed Bias Stress Conditions Mechanism," 2004 IRPS, Phoenix, AZ, 2004.

B. Zhu, J. S. Suehle, and J. B. Bernstein, "Mechanism of Dynamic NBTI of pMOSFETs," Proceedings IEEE Integrated Reliability Workshop, Oct 18-21, 2004.

E. M. Vogel and D. Heh, "Depth profiles of electrically active defects in high- $\kappa$  gate stacks using charge pumping," *Advanced Gate Stack Engineering working Group Biannual Meeting*, Austin Texas, 2005.

D. Heh, E. M. Vogel, and J. B. Bernstein, "New Insights into the Polarity Dependence of Threshold Voltage Shifts During Constant Voltage Stress," *IEEE Electron Device Letters*, submitted.

D. Heh, E. M. Vogel, and J. B. Bernstein, "New Insights into Threshold Voltage Shifts for Ultrathin Gate Oxides," in *Integrated Reliability Workshop final report*, pp. 99-101, 2004.

D. Heh, E. M. Vogel, and J. B. Bernstein, "Impact of substrate hot hole injection on ultrathin silicon dioxide breakdown," *Appl. Phys. Lett.*, vol. 82, pp. 3242-3244, 2003.

J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. Heh, and J. S. Suehle, "Energy distribution of interface traps in high- $\kappa$  gated MOSFETs," in *Dig. Symp. VLSI Technology*, pp. 161-162, 2003.

J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. W. Heh, J. S. Suehle, "Asymmetric Energy Distribution of Interface Traps in n- & p- MOSFETs with HfO<sub>2</sub> Gate Dielectric on Ultra-thin SiON Buffer Layer," *IEEE, Electron Device Letters*, Vol. 25, No. 3, pp. 126-128 (March 2004).

# NANOELECTRONIC DEVICE METROLOGY

## GOALS

The overall goal of the Nanoelectronic Device Metrology (NEDM) task is to develop the metrology that will help enable new nanotechnologies (such as Si-based quantum devices, molecular electronics) to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices. Two related goals are the optimization of Si-based single-electron devices for one-electron logic, and the development of ultra-sensitive nanotransistor devices to observe charge reconfigurations in biological systems. Another targeted goal is to develop test structures and methods to measure the electrical properties of small ensembles of molecules reliably (see Fig. 1).



Figure 1. Curt Richter loads a molecular electronic sample for electrical characterization.

## CUSTOMER NEEDS

The CMOS FET (Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) shows no known solutions in the short term for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to

augment and/or replace standard planar CMOS devices. Two promising beyond-CMOS technologies that each take a very different fabrication approach are molecular electronics and Si-based quantum electronic devices. Molecular electronics is based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches used in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. Alternatively, research and development for silicon-based nanoelectronics (*e.g.*, Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology. Finally, there is a large potential set of customers for ultra-sensitive charge electrometry of biological systems. Many diseases result from changes in protein structure or folding. We will investigate whether such changes can be elucidated through capacitive coupling to nearby nanotransistors.

In all these cases, our project has the capability to offer early guidance to these emerging fields and to assist companies in pursuing productive areas and rejecting problematic ones. Because these fields are not yet mature, as our relatively moderate efforts progress, they can yield large payoffs for the customers.

## TECHNICAL STRATEGY

- Develop the electrical and physical metrology of Si-based nanoelectronics. The focus is on the basic building blocks of silicon quantum electronic devices (*e.g.*, quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.

**DELIVERABLES:** Complete systematic investigation of carrier mobility in Si-nanowire FETs nanofabricated from SOI wafers; prepare and submit manuscript.  
1Q 2005

## Technical Contacts:

Curt A. Richter  
Eric M. Vogel  
Neil M. Zimmerman

**DELIVERABLES:** Report process flow and characterization of prototypical enhancement-mode Si-nanowire FETs based upon Schottky-barrier contacts; prepare and submit manuscript. 3Q 2005

- Develop geometries and architectures that maximize flexibility and operating temperature of single-based single-electron devices.

**DELIVERABLES:** Complete and publish an experimental and theoretical study comparing charge offset drift in metal-based and Si-based SET transistors and/or the static charge offset problem in Si-based SET transistors. 1Q 2006

- Develop robust molecular test structures in order to use them to measure the electrical properties of molecules. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used to determine charge conduction mechanisms and in the validation of predictive theoretical models (see Fig. 2 and Fig. 3).

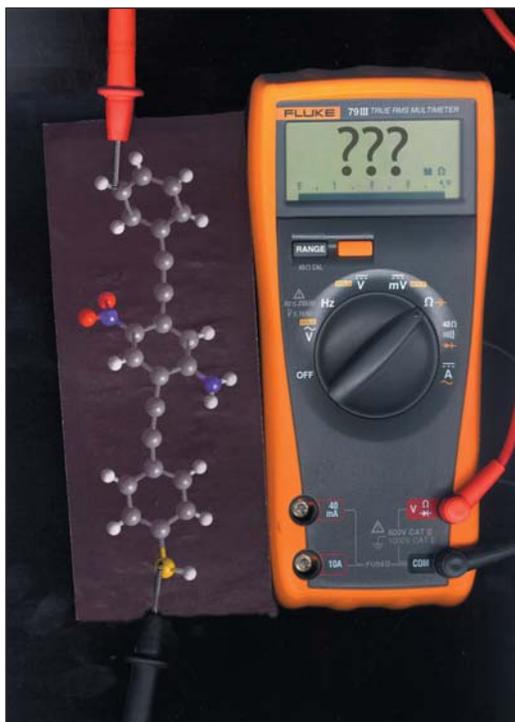


Figure 2. The concept behind molecular electronic test structures.

**DELIVERABLES:** Develop and demonstrate FTIR-based technique to characterize top-metal/molecular interfaces. Investigate initial metal/molecule interfaces. Prepare and submit manuscript. 3Q 2005

**DELIVERABLES:** Develop a “nano-gap capacitor” to characterize charge polarization in molecular electronic molecules. 2Q 2006

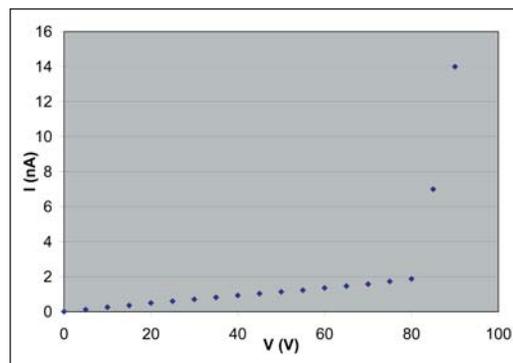


Figure 3. Air breakdown measurement in a capacitor with a gap of  $1 \mu\text{m}$ . The gap is deduced from the capacitance value. The sharp increase in current shows the start of air breakdown at about  $80 \text{ V}$  across the capacitor. Note that the gap of  $1 \mu\text{m}$  is about equal to the mean free path of electrons in air at room temperature, so that this result does not lie on the standard Paschen curve.

- Determine the ultra-sensitive charge electrometry capabilities of Si-nanotransistors through measuring the sensitivity and its relationship to device structure. A longer term strategy is to assess how the sensitivity is affected by biological structures in solution (see Fig. 4).

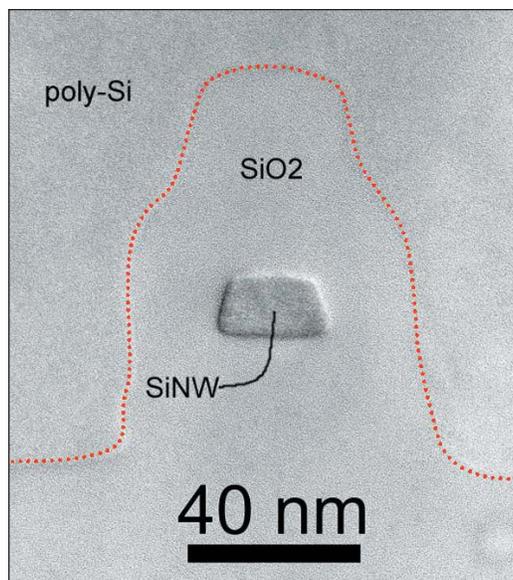


Figure 4. Si nanowire field-effect transistor.

## ACCOMPLISHMENTS

- *Enhanced Inversion Mobility in Silicon Nanowire Field Effect Transistors Demonstrated.* Dr. Sang-Mo Koo and colleagues have demonstrated that silicon nanowire (SiNW) field effect transistors (FETs) fabricated by a standard ‘top-

down' approach exhibit substantially enhanced transport performance. A systematic study on the inversion electron transport properties of SiNWs with different channel geometries has shown that a SiNW device exhibits enhanced inversion channel current density: the extracted electron inversion mobility of the 20 nm width nanowire channel ( $1000 \text{ cm}^2/\text{Vs}$ ) is found to be two times higher than that of the reference MOSFET of large dimension ( $W > 1 \text{ }\mu\text{m}$ ). The enhancement is attributed to the possible suppression of inter-valley phonon scattering due to strain in SiNW caused by the oxidation process. As the feature sizes of FETs are scaled downward, the semiconductor industry is working to meet the increasing challenges of nanoscale devices that are smaller and yet can be manufactured with minimal deviation from today's standard manufacturing processes. These results strongly suggest that lithographically fabricated SiNW FETs, which are compatible with Si ULSI technology, can bring about significant performance benefits in nanoscale electronics, preserving the basic silicon technology infrastructure upon which current industry relies.

■ *Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors.* We have shown that SiNWs with Schottky contacts can be used as enhancement-mode FETs with an excellent on/off current ratio. The process does not require any source and drain doping or silicide formation, thereby allowing for a simple process without thermal annealing. Silicon nanowire field-effect transistors (SiNWFETs) were fabricated with a highly simplified integration scheme to function as Schottky barrier transistors with excellent enhancement-mode characteristics and a high on/off current ratio  $\sim 10^7$ . SiNWFETs show significant improvement in the thermal emission leakage ( $\sim 6 \times 10^{-13} \text{ A}/\mu\text{m}$ ) compared to reference FETs with a larger channel width ( $\sim 7 \times 10^{-10} \text{ A}/\mu\text{m}$ ). The drain current level depends substantially on the contact metal work function as determined by examining devices with different source-/drain-contacts of Ti ( $\approx 4.33 \text{ eV}$ ) and Cr ( $\approx 4.50 \text{ eV}$ ). The different conduction mechanisms for accumulation- and inversion-mode operation were determined and confirmed by comparison with two-dimensional numerical simulation results. Schottky barrier FETs are of great interest in their own respect as an alternative to traditional doped source and drain device structure, because sub-100-nm range scaling encounters fundamental problems including high leakage current and parasitic resistance. Schottky barrier FETs have

a number of advantages including simple and low-temperature processing, good suppression of short-channel effects, and the elimination of doping and subsequent activation steps. These features are particularly desirable for SiNW devices because they can circumvent difficult fabrication issues such as an accurate control of the doping type/level and the formation of reliable ohmic contacts (see Fig. 5).

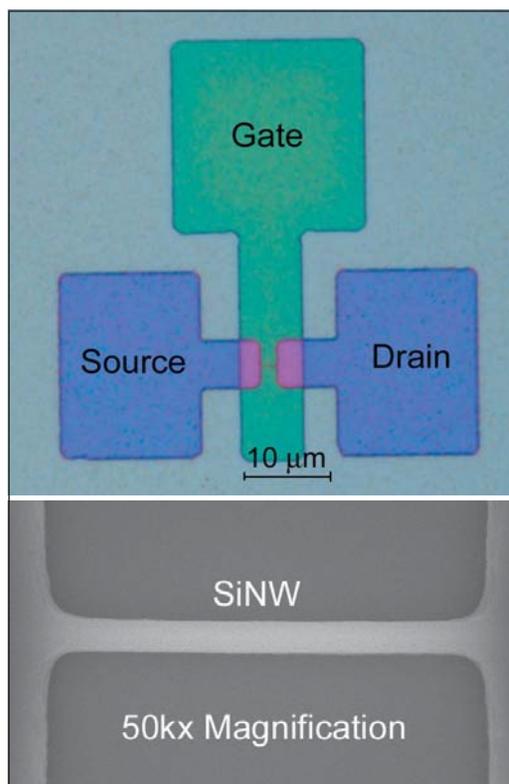


Figure 5. A SiNWFET based upon Schottky-barrier source/drain contacts.

■ *Joint NIST/HP Research Progresses Toward Critical Molecular Electronics Measurements.* Research at the NEDM and Hewlett Packard (HP) Laboratories is progressing toward reliable methods for measuring the electrical behavior of molecular electronic devices, an emerging nanotechnology eyed for future integrated circuits. By using a crossbar test structure consisting of a molecular monolayer sandwiched between a series of perpendicular metal wires, collaborators at separate facilities recorded nearly identical electrical measurements. This step, along with others taken to eliminate potential sources of error, ensures that the measured behavior is directly attributable to the device and not the experimental setup. Electrical (current-voltage, or IV) measurements

of crossbar devices containing eicosanoic acid exhibit a controllable, two-state switching behavior that is due to the presence of the molecular layer. However, the molecular monolayer is not the sole cause. Rather, the switch-like behavior most likely arises from the interaction of the molecules with the electrodes. This example illustrates that the properties of molecular electronic devices are often determined not by the molecule alone, but by the entire device that consists of both the molecules and the attachment electrodes. This two-state behavior was independently measured in two separate laboratories, indicating that it is not a measurement artifact and illustrating that these devices are robust enough to ship via conventional methods and remain active. In addition to IV measurements, what will may be the first capacitance-voltage (CV) measurements of molecular monolayer-based devices were taken at NIST. These CV curves also show two-state behavior.

■ *Novel approach to investigate buried metal-organic interfaces for molecular electronics.* We have developed and used a novel approach to investigate the top metal contact in metal-organic monolayer devices. In the emerging arena of molecular electronics, detailed characterization of organic monolayers encapsulated between two electrodes is necessary to correlate the electrical responses of molecular devices with the fundamental physical properties of the monolayers. The technique developed at NIST takes advantage of the natural infrared transparency of Si wafers to enable vibrational characterization of monolayer films after deposition of a technologically relevant metal electrode. The samples as prepared encapsulate the organic layer in exactly the same manner as fully fabricated devices. IR and electrical samples were fabricated simultaneously, allowing direct comparison of the spectroscopic results with electrical device performance. Two different chemical processes were utilized to attach nm-thick alkane films to the Si substrates: a conventional silanization process for films on thin oxides and a novel process previously optimized at NIST for direct attachment to silicon. Molecules on silicon are of interest as active electronic layers and for surface engineering. Monolayers bound directly to silicon are expected to have less interfacial capacitance than those on oxides, be more amenable to further processing, and be resistant to degradation due to the nature of the strong covalent bond. Results were presented at the 7<sup>th</sup> International Molecular Electronics conference

and a manuscript was submitted to the journal *Nanoletters*.

## FY OUTPUTS

### COLLABORATIONS

NTT, Akira Fujiwara, Si-nanowire metrology

Hewlett-Packard, R. Stanley Williams et al., Interface properties of molecular electronic test structures

NIST Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures

### RECENT PUBLICATIONS

Richter, C.A., D.R. Stewart, D.A.A. Ohlberg, R.S. Williams; "Electrical Characterization of Al/AlO<sub>x</sub>/Molecule/Ti/Al Devices," *Appl. Phys. A* 2005, 80, 1355–1362. (March 2005)

Hacker, C.A.; Anderson, K.A.; Richter, L.J.; Richter, C.A.; "Comparison of Si-O-C interfacial bonding of alcohols and aldehydes on Si(111) formed from dilute solution with ultraviolet irradiation" *Langmuir* **21**(3), 882-889 (2005).

Koo S.-M., A.-F. Fujiwara, J.-P. Han, E. Vogel, C. Richter, and J. Bonevich, "High Inversion Current in Silicon Nanowire Field Effect Transistors" *Nano Lett.*, Vol. 4, 2107-2111, Nov. 2004.

Richter L. J., C. S. Yang, P. T. Wilson, C. Hacker, R. D. van Zee, J. J. Stapleton, D. L. Allara, J. M. Tour, "Optical Characterization of Oligo(phenylene-ethynylene) Self-Assembled Monolayers on Gold," *J. Phys. Chem. B.*, Vol. 108, No. 33, pp. 12547-12559 (19-AUG-2004).

Hacker C.A., J. D. Batteas, J. C. Garno, M. Marquez, C. A. Richter, L. J. Richter, R. D. van Zee, C. D. Zangmeister, "Structure and Chemical Characterization of Self-Assembled Mono-Fluoro-Substituted Oligo(phenylene-ethynylene) Monolayers on Gold," *Langmuir*, Vol. 20, No. 15, pp. 6195-6205 (22-JUN-2004).

Richter C. A., C. Hacker, L. J. Richter, E. M. Vogel, "Molecular Devices Formed by Direct Monolayer Attachment to Silicon," *Solid State Electronics*, Vol. 48, pp. 1747-1752 (17-JUN-2004).

# POWER SEMICONDUCTOR DEVICE METROLOGY

## GOALS

The goals of the project are to develop electrical and thermal measurement methods and equipment in support of the development and application of advanced power semiconductor devices.

## CUSTOMER NEEDS

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient long distance high voltage power transmission. Rapid technical advances are occurring in the development of new power semiconductor materials and designs to address these needs. With the introduction of these new materials and designs comes new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the introduction of SiC power Schottky diode products in the 400 V to 1200 V range and led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 15 kHz power switching capability.

*“In 2004, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: “his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in ... more efficient/compact power supplies, and higher efficiency power distribution/transmission systems.”*

Several industry and government programs are currently underway to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE)

is to develop half-bridge modules with 15 kV, 110 A, 20 kHz capability in the next few years. The emergence of HV-HF devices with such capability is expected to revolutionize utility and military power distribution and conversion by extending the use of Pulse Width Modulation (PWM) technology, with its superior efficiency and control capability, to high voltage applications.

The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which include advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements. In addition, HV-HF power devices are an enabling technology for alternative energy sources and storage systems. The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements.

## TECHNICAL STRATEGY

The strategy is to support the measurement infrastructure of the semiconductor industry by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of devices and ICs. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters to aid in application insertion. NIST is taking a lead role in developing the device metrology and performance metrics necessary for both the DARPA and EPRI efforts and the new industries envisioned by these programs. NIST is also pioneering electrical and thermal measurement methods for HV-HF devices.

*[The Project] ... continues to lead industry needs by providing state-of-the-art capability for the measurement of unique power device characteristics at critical operating conditions.”*

*NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003*

**Technical Contact:**  
A. Hefner

## PERFORMANCE, RELIABILITY, AND APPLICATION CHARACTERIZATION FOR DARPA-WBST-HPE DEVICES AND MODULE PACKAGES

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable Solid State Power Substations (SSPS) for future Navy warships. Current distribution approaches being considered for the next generation of aircraft carriers and destroyers employ a 13.8 kV AC power distribution that is stepped down to 450 V AC by using large (6 ton and 10 m<sup>3</sup>) 2.7 MVA transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the Phase 2–3 program for 2005 through 2008.

### METROLOGY FOR MAPPING SiC POWER BIPOLAR DEVICE DEGRADATION

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for bipolar structures is an observed degradation in the electrical characteristics over time. The degradation occurs from latent defects such as Basel Plane Dislocations that result in the formation and growth of stacking faults activated by excess carrier recombination. The defects cause severe current nonuniformities to occur, resulting in on-state voltage, switching, and thermal performance degradation.

**DELIVERABLE:** Develop automated stress and degradation monitoring systems to assess degradation of SiC devices after 10,000 hours of operation. 4Q 2005

**DELIVERABLE:** Utilize NIST one-of-a-kind high speed thermal image measurements to characterize SiC power diode conduction uniformity performance before and after stress conditions and correlate results with light emission stacking fault measurements (with NRL). 4Q 2005

### METROLOGY FOR NONDESTRUCTIVE SWITCHING FAILURE

Power devices undergo their greatest electro-thermal stress under switching conditions. There are

a number of known catastrophic failure mechanisms that occur as a device is switched off with an inductive load. NIST has developed a nondestructive system to test for the failure limits under inductive switching, has done extensive research on Si device failure limits, and will extend that work to include SiC power devices.

**DELIVERABLE:** Perform unclamped inductive switching measurements for SiC MOSFETs and IGBTs produced by DARPA WBG program. 4Q 2005

### CIRCUIT SIMULATOR MODELS FOR SiC POWER SWITCHING DEVICES

Parameter extraction is a critical component in developing and using device models in circuit and system simulations and in establishing performance benchmarks for new device technologies. For new devices, not only must new models be developed, but methods must be modified and new ones developed for extracting the parameters for the models.

**DELIVERABLE:** Utilize NIST IMPACT model parameter extraction tools to characterize SiC power MOSFETs and IGBTs introduced by the DARPA WBST-HPE program. Provide models for use in simulating SSPS. 4Q 2005

### ACCOMPLISHMENTS

- *Extended capabilities of IMPACT parameter extraction software.* The capabilities of the parameter extraction software, *IMPACT*, were extended to include MOSFETs (in addition to IGBTs) and three prototypes of SiC material (in addition to Si). This was done in collaboration with the University of Puerto Rico, Mayaguez, and two SURF (Summer Undergraduate Research Fellow) students.

- *High voltage curve tracer and reverse recovery systems.* The development of a 25 kV variable pulse width curve tracer for both 2 and 3 terminal devices was completed. Safety protection and an interlock system have been tested and qualified. A high voltage reverse recovery test system with 3 kV, 15 A capability was also developed. These systems are critical components in the SiC power semiconductor device metrology tasks.

- *Played a major role in planning and evaluating progress of DARPA Wide Bandgap Power Device program.* Developed the metrology, measured device deliverables to government from DARPA contractors, and used NIST data to provide assessment of program to DARPA director.

- *Initiated new program with EPRI to develop solid state power distribution transformers using ultra high voltage semiconductor devices.* The goal is to replace all existing power distribution transforms with Intelligent Universal Transformers that provide better control of the power grid, provide power factor correction at point of use, improve power quality, and enable plug-and-play insertion of alternate energy sources. NIST aided in mapping existing power semiconductor technologies for this application and in establishing an EPRI road map for development of ultra-high-voltage semiconductor devices.

- *Played a major role in initiating and planning a new DARPA/Navy SiC shipboard power distribution program.* The program involves insertion of power distribution technologies enabled by ultra-high-voltage semiconductor devices into next generation more electric Navel carrier, destroyer, and submarine platforms.

- *Completed development of SiC power MOSFET model and completed development of IMPACT extraction tools for SiC power device model parameter extraction.* Performed parameter extraction for SiC MOSFETs produced by DARPA WBG program and validated simulations.

- A paper with Al Hefner as lead author and including other NIST authors David Berning, Colleen Ellenwood, and Adwoa Akuffo won the William M. Portnoy Award. This paper was presented by David Berning at the IEEE 39<sup>th</sup> Annual Meeting of the Industry Applications Society in October 2004. The award is issued by the Power Electronics Devices and Components Committee, and is recognition for both the paper and the presentation. The title of the paper is "Characterization of SiC PiN Diode Forward Bias Degradation" by Allen Hefner, Ty McNutt, Adwoa Akuffo, Ranbir Singh, Colleen Ellenwood, Dave Berning, Mrinal Das (CREE), Joseph Sumakeris (CREE), and Robert Stahlbush (NRL).

## FY OUTPUTS

### COLLABORATIONS

Avanti Inc., Parameter extraction for IGBT library component models

Avanti Inc./University of Arkansas, SiC power device modeling

Avanti Inc./UPRM, Characterization and modeling of electronic packages for thermal model library component models

NIST Division 812, Electronic Materials Characterization Project/Advanced MOS Device Reliability and Characterization Project, Benchmarks for quantum-mechanical device simulation

NIST/CREE, Development of SiC MOSFET electro-thermal model

Participants for DARPA contract (including NRL, ARL, Virginia Tech, CREE, University of Arkansas, Rockwell, etc.), Wide bandgap power device program

Rockwell Science Center/NIST, Development of SiC transistor models

University of Maryland, Metrology for multi-technology System-on-a-Chip (SoC)

Virginia Polytechnic Institute and State University, SiC power device utilization

## EXTERNAL RECOGNITION

Allen R. Hefner, elected IEEE Fellow "for contributions to the theory and modeling of power semiconductor devices"

## RECENT PUBLICATIONS

Allen Hefner, Ty McNutt, Adwoa Akuffo, Ranbir Singh, Colleen Ellenwood, Dave Berning, Mrinal K. Das, Joseph J. Sumakeris, and Robert Stahlbush, "Characterization of SiC PiN Diode Forward Bias Degradation," Volume: 2, 3-7 Oct. 2004, Pages:1252-1260.

J. Reichl, D. Berning, A. Hefner, and J-S. Lai, "Six-Pack IGBT Dynamic Electro-Thermal Model; Parameter Extraction and Validation," IEEE Applied Power Electronics Conference, Anaheim, CA, Feb. 2004.

R. Singh, A. R. Hefner Jr., "Reliability of SiC MOS Devices," Journal of Solid-state Electronics, Vol. 48, No. 10-11, pp. 1717-1720 (24-JUNE-2004).

T. R. McNutt, A. R. Hefner Jr., A. Mantooth, J. Duliere, D. W. Berning, R. Singh, "Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator," IEEE Trans. Power Electronics, Vol. 19, No. 3, pp. 573-581 (01-MAY-2004).

D. W. Berning, J. V. Reichl, A. R. Hefner Jr., M. Hernandez, C. H. Ellenwood, J. Lai, "High Speed IGBT Module Transient Thermal Response Measurements for Model Validation," Proc., IEEE Industry Applications Society (IAS) Annual Meeting, Oct. 12-16, 2003, Salt Lake City, Utah, pp. 1826-1832 (12-OCT.-2003).

X. Huang, P. Elton, J. Lai, A. R. Hefner Jr., D. W. Berning, S. Chen, T. Nehl, "EMI Characterization with Parasitic Modeling for a Permanent Magnet Motor Drive," Proc., IEEE Industry Applications Society (IAS) Annual Meeting, Oct. 12-16, 2003, Salt Lake City, Utah, pp. 416-423 (12-OCT.-2003).

T. R. McNutt, A. R. Hefner Jr., A. Mantooth, D. W. Berning, S. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," Proc., Power Electronics Specialist Conference, Power Electronics Specialist Conference, Aca pulco, Mexico, 10 p. (11-JUNE-2003).

R. Singh, K. G. Irvine, D. C. Capell, J. T. Richmond, D. W. Berning, A. R. Hefner Jr., J. W. Palmour, "Large Area, Ultra-high Voltage 4H-SiC PiN Rectifiers," IEEE Trans. Electron Devices, Vol. 49, No. 12, pp. 2308-2316 (01-DEC.-2002).

R. Singh, D. C. Capell, A. R. Hefner Jr., J. Lai, J. W. Palmour, "High-Power 4H-SiC JBS Rectifiers," IEEE Trans. Electron Dev., Vol. 49, No. 11, pp. 2054-2063 (01-NOV.-2002).

J. J. Rodriguez, J. V. Reichl, Z. R. Parrilla, A. R. Hefner Jr., D. W. Berning, M. Velez-Reyes, J. Lai, "Thermal Component Models for Electro-Thermal Analysis of Multichip Power Modules," Proc., 2002 IEEE Industry Application Society, IEEE Industrial Applications Society Meeting, Oct. 13-18, 2002, Pittsburgh, Pennsylvania, pp. 234-241 (24-OCT.-2002).

# ORGANIC ELECTRONICS METROLOGY

## GOALS

Organic electronic devices are increasingly being incorporated into electronics packaging and are projected to revolutionize integrated circuits through new applications that take advantage of low-cost, high-volume manufacturing, nontraditional substrates, and designed functionality. A critical need exists for new diagnostic probes, tools, and methods to address new technological challenges. Their adoption will be advanced considerably by the development of an integrated and interdisciplinary suite of metrologies to correlate device performance with the structure, properties, and chemistry of critical materials and interfaces. NIST will guide the development of standard test methods and provides the fundamental measurements needed for the rational and directed development of materials and processes to realize the potential of organic electronics.

## CUSTOMER NEEDS

An exciting array of new devices and applications are now possible with the development of electronic devices using organic materials because they are amenable to low-cost, high-volume manufacturing, incorporation on flexible substrates, and designed functionality (Fig. 1). Completely new technologies are under development including printable large-area displays, wearable electronics, paper-like electronic newspapers, low-cost photovoltaic cells, ubiquitous integrated sensors, and radio-frequency identification tags. At this stage, new materials and processes are evolving rapidly to optimize device performance, ease processing limitations, and demonstrate frontier applications. However, systematic progress in organic electronics is challenging because of the enormous range of potential materials (from polymers to nanocomposites) and manufacturing methods (roll-to-roll printing, fluidic self-assembly, micro-contact printing, laser ablative printing, and ink-jet printing).

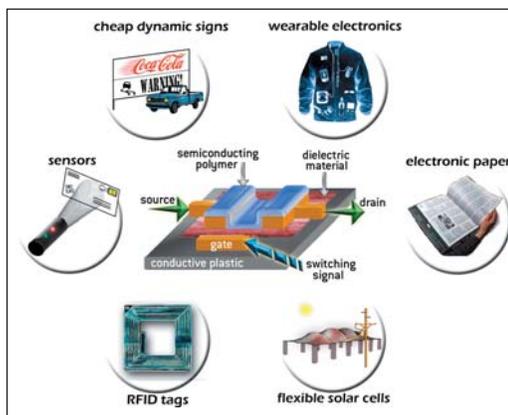


Figure 1. Schematic representation of potential organic electronics applications.

A key technical barrier is the lack of correlation between device performance and the structure, properties, and chemistry of critical materials and interfaces. Without this knowledge, guided improvements in materials and processing design are not possible and meaningful standard test protocols cannot be developed. Characterizing the chemically complex (mostly carbon-based) soft interfaces found in organic devices is critical to proper interpretation of charge transport through molecules rather than single crystal structures. Identifying individual contributions to performance variations requires metrology unavailable to device manufacturers and spanning multiple disciplines: device physics, material electronic structure, chemistry, and materials science.

## TECHNICAL STRATEGY

The initial focus of the NIST program is on the organic field effect transistor (OFET) because, as in the silicon industry, the transistor is the basic building block for active devices. The fundamental framework, characteristics, and issues that arise during OFET development are transferable to other organic electronic devices because of commonalities in architecture and interfaces. NIST is engaged in complementary activities to address the primary technical barriers facing the adoption of organic electronics: 1) unique measurements of organic materials and interfaces for both a) structure and chemistry and b) electronic properties; and 2) the development of an integrated measurement test platform to correlate device performance with the structure and properties of

## Technical Contacts:

Eric Lin  
Dean DeLongchamp  
Jan Obrzut  
Curt Richter  
Lee Richter  
Daniel Fischer

active organic materials. This test platform can also be used to transfer measurement technology to device development laboratories.

1. Interfacial structure and chemistry fundamentals: The basic OFET consists of thin layers (30 nm to 60 nm thick) of disparate materials including the organic semiconductor, dielectric, interconnect, electrode, and substrate. OFET performance and operational stability critically depend upon charge transport and material interactions between inorganic and organic materials, particularly at semiconductor/dielectric and semiconductor/metal interfaces. Detailed interfacial structure information (electronic structure, molecular orientation, interfacial roughness, interfacial chemistry), correlated with electronic properties is required to predict performance.

We are developing a suite of powerful measurement methods including X-ray, neutron, and optical probes capable of *in-situ* nondestructive characterization of critical organic interfaces. Changes in interfacial structure, chemistry, and orientation are correlated with OFET device evaluation. Near-edge X-ray Absorption Fine Structure (NEXAFS) spectroscopy and nonlinear optical techniques are ideally suited for nondestructive characterization of organic interfaces for chemistry, orientation, and structure. NEXAFS can distinguish chemical bonding in the light elements, measure the orientation of interfacial molecules, and separately measure surface versus bulk chemistry simultaneously. Second order nonlinear optical spectroscopies, such as sum frequency generation (SFG), are particularly appropriate for probing the buried semiconductor/dielectric interface. Interfacial structure (width, roughness) between OFET layers must also be measured in order to interpret performance variations. X-ray and neutron reflectometry are powerful thin film characterization methods for determination of the interfacial profile between layers.

**DELIVERABLES:** Develop measurement protocols and analysis tools to quantify confidence levels in molecular orientation and chemical conversion with NEXAFS spectroscopy. 4Q 2004

**DELIVERABLES:** NEXAFS measurements of chemical conversion, molecular orientation, and defect density of soluble oligothiophenes with varying number of repeat units. 2Q 2005

**DELIVERABLES:** Complete FTIR, UV-Vis, and spectroscopic ellipsometer measurements of the structural changes in P3HT films induced by annealing above the melt temperature. 3Q 2005.

**DELIVERABLES:** Complete NEXAFS measurements of evaporated small molecules onto silicon surfaces as a function of film thickness and deposition temperature. 4Q 2005

2. Electronic property fundamentals: The response of organic electronic materials to electrical fields must also be measured to separate device architecture artifacts and intrinsic material properties. Model sandwich test structures have been designed to individually test the frequency response of semiconducting and dielectric materials employed within organic electronic ensembles. Capacitance and conductance measurements will be performed at frequencies up to 12 GHz to determine the dielectric properties of these materials. These results will be compared with traditional metrics such as current or capacitance versus voltage curves as functions of temperature, layer thickness, or contact metals. With new information (electronic and interfacial), we will elucidate mechanisms underlying the many anomalous phenomena observed in OFETs, such as permanent bias instability and the true nature of carrier mobility distribution, both of which are opaque to traditional metrics.

**DELIVERABLES:** Construct samples and evaluate feasibility of frequency measurements of P3HT. 1Q 2005

**DELIVERABLES:** Measure the electrical properties of conductive polymer dispersions such as Poly(3,4-ethylene dioxythiophene) : poly(styrene sulfonic acid) (PEDOT:PSS) as a function of processing. 2Q 2005.

3. Integrated measurement platform: To directly compare OFET performance with its interfacial structure and chemistry, test structures have been fabricated on a single substrate that will include both active devices and pre-defined measurement regions. By employing our methods using these custom platforms, we will identify motifs that develop after processing and during operation that critically affect OFET performance. The use of an integrated substrate removes variations that may affect measurements performed separately. Specific test structures optimized to transfer information to industrial laboratories will be developed. We plan to provide electrical measurement protocols that will identify electronic signatures representative of performance-influencing structural changes and meaningful standard test methods.

**DELIVERABLES:** Design and fabricate OFET test structures with varying channel lengths and widths. 4Q 2004

**DELIVERABLES:** Measure field effect hole mobility, threshold voltage, and on/off ratios for P3HT OFETs spin-cast onto the test structure. 2Q 2005

**DELIVERABLES:** Evaluate correlations between structural measurements and device performance of P3HT films prepared with varying solvents or with varying spin-coating speeds. 4Q 2005

## ACCOMPLISHMENTS

■ Near-edge X-ray absorption fine structure (NEXAFS) spectroscopy was applied to several classes of organic electronics materials to investigate the electronic structure, chemistry, and orientation of these molecules near a supporting substrate. In collaboration with the University of California-Berkeley, NEXAFS spectroscopy was used successfully to quantify the simultaneous chemical conversion, molecular ordering (Fig. 2), and defect formation of soluble oligothiophene precursor films for application in organic field

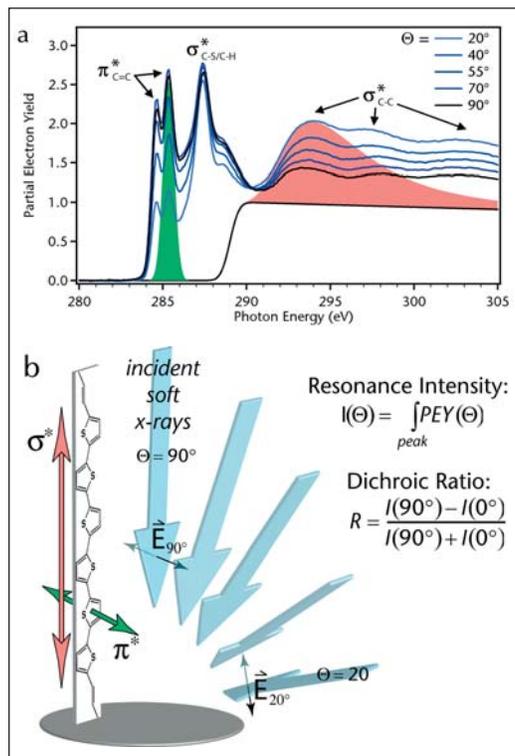


Figure 2. a, NEXAFS carbon K-edge spectra collected at changing incident angles from a film annealed at 200 °C. The green area indicates the oligothiophene  $\pi^*$  resonance used to determine planar orientation while the pink area indicates the  $\sigma^*$  resonance used to determine long axis orientation. b, Image depicting the orientation and spatial orientations of its primary K-edge carbon resonances. Blue arrows indicate incident polarized soft X-rays with electric field vectors extending normal to the plane of photon polarization.

effect transistors. Variations in field-effect hole mobility with thermal processing are directly correlated to the orientation and distribution of molecules within 3 nm to 20 nm thick films.

■ Poly(3,4-ethylene dioxythiophene): poly(styrene sulfonic acid) (PEDOT:PSS) films, a conductive polymeric material, exhibit a complex structure of interconnected conductive PEDOT domains in an insulating PSS matrix that controls its electronic properties. This structure is affected by a water rinse, which removes a large quantity of PSS with negligible PEDOT loss. Upon PSS removal, film thickness is reduced by 35 %, the film DC conductivity is increased by 50 %, and a prominent AC relaxation is eliminated. These results show that the removed PSS is unassociated with the PEDOT and that the interconnected conductive domains are not substantially altered by the removal of a significant fraction of the insulating material. However, the facile removal of acidic PSS may benefit organic light emitting diode fabrication by reducing acid attack on transparent electrodes and lead to more robust performance in switching circuits from the extension of the working frequency range.

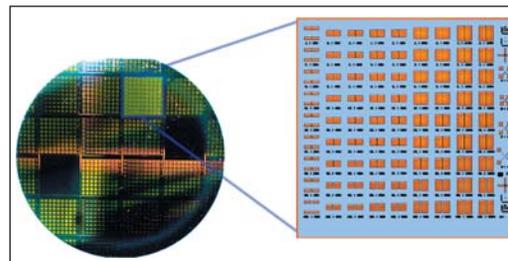


Figure 3. Photo of an organic field effect transistor (OFET) test bed designed and fabricated at NIST. The test bed consists of bottom contact transistors on a silicon dioxide dielectric with a doped silicon wafer as the gate. The structure includes variations in channel length and width as well as large open areas for structural characterization.

■ Organic FET test structures have been designed and fabricated onto silicon wafers with variations in transistor channel length and channel width (Fig. 3). Devices constructed using organic semiconductors such as poly(3-hexyl thiophene) (P3HT) have been tested for their electrical characteristics such as the field effect hole mobility, on/off ratios, and threshold mobilities. Variations in mobility, for example, are observed with changes in processing variables such as annealing temperature and casting solvent. Ongoing studies are focused on correlations between the microstructure of P3HT and device performance.

## COLLABORATIONS

Polymers Division, MSEL – C. K. Chiang, Oleksiy Anopchenko, Kenji Kano, Brandon Vogel, Youngsuk Jung, R. Joseph Kline, Bryan D. Vogt, Hae-Jeong Lee, Wen-li Wu

Semiconductor Electronics Division, EEEL – Oleg Kirillov, Eric Vogel

Ceramics Division, NIST – Daniel A. Fischer, Sharadha Sambasivan

Surface and Microanalysis Science Division, CSTL – Marc Gurau

Center for Neutron Research, NIST –Sushil K. Satija, Derek Ho

Vitex – Nicole Rutherford, L. Moro

University of California, Berkeley – Amanda Murphy, Paul Chang, Jean Frechet, Vivek Subramanian

Stanford University – Mang-mang Ling, Zhenan Bao

Xerox – Liang Li, Beng Ong, Michael Chabinye

## RECENT PUBLICATIONS

D. M. DeLongchamp, S. Sambasivan, D. A. Fischer, E. K. Lin, P. Chang, A. R. Murphy, J. M. J. Fréchet, V. Subramanian, “Direct correlation of organic semiconductor film structure to field-effect mobility,” *Advanced Materials*, in press (2005).

D. M. DeLongchamp, B. D. Vogt, C. M. Brooks, K. Kano, J. Obrzut, C. A. Richter, O. Kirillov, E. K. Lin, “Influence of a water rinse on the structure and electrical properties of poly(3,4-ethylene dioxythiophene):poly(styrene sulfonic acid) films,” submitted to *Langmuir* (2005).

J. Obrzut and K. Kano, “Impedance and Non-Linear Dielectric Testing at High Ac Voltages Using Waveforms,” accepted to *IEEE Transactions on Instrumentation and Measurement* (2005).

A. R. Murphy, P. VanDyke, J. Liu, J. M. J. Fréchet, P. C. Chang, V. Subramanian, D. M. DeLongchamp, S. Sambasivan, D. A. Fischer, E. K. Lin, “Investigation of a Series of High Mobility Solution-Processed Ultrathin Oligothiophene Films,” submitted to *JACS* (2005).

B. D. Vogt, V. M. Prabhu, C. L. Soles, S. K. Satija, E. K. Lin, and W. L. Wu, “Control of moisture at buried interfaces through substrate surface modification,” *Langmuir*, in press (2005).

J. Obrzut and A. Anopchenko, “Input Impedance of a Coaxial Line Terminated with a Complex Gap Capacitance - Numerical and Experimental Analysis” *IEEE Transactions on Instrumentation and Measurement*, **53**: 1197-1201 (2004).

# NIST ADVANCED MEASUREMENT LABORATORY NANOFAB

## GOALS

The NIST Advanced Measurement Laboratory (AML) Nanofab will:

- enable fabrication of prototypical nanoscale test structures, measurement instruments, standard reference materials, electronic devices, MEMS, and bio-devices critical to NIST's Strategic Focus Areas (Nanotechnology, Homeland Security, Healthcare) and the Nation's Nanotechnology Needs
- provide access to expensive nanofabrication tools, technologies and expertise in a shared-access, shared-cost environment to NIST and its partners
- foster internal collaboration in Nanotechnology across NIST's Laboratories
- foster external collaboration in Nanotechnology with NIST's partners.

## CUSTOMER NEEDS

To continue to respond to U.S. science and industry's needs for more sophisticated measurements and standards in the face of heightened global competition, NIST is constructing one of the most technologically advanced facilities in the world—the Advanced Measurement Laboratory, or AML. The NIST Nanofab (Fig. 1) is one of five buildings in the AML at the Gaithersburg, MD campus. The AML Nanofab will provide researchers at NIST working on a variety of semiconductor and other nanotechnology research the ability to fabricate prototypical nanoscale test structures, measurement instruments, standard reference materials, and electronic devices.

## TECHNICAL STRATEGY

The AML contains two above ground instrument buildings, two completely below ground metrology buildings, and one Class 100 clean room building that will house the NIST AML Nanofab. The AML will provide NIST with superior vibration, temperature and humidity control, and air cleanliness. The NIST AML Nanofab has approximately 1000 m<sup>2</sup> of Class 100, raised floor, bay and chase, clean room space. NIST has invested in a complete suite of new equipment (capable of processing 150 mm wafers) that will be installed over the upcoming year. This includes

furnaces (two banks of four tubes each), LPCVD (poly, nitride, LTO), rapid thermal annealer, four reactive ion etchers (SF<sub>6</sub>/O<sub>2</sub>, FI Metal, CI Metal, Deep), five metal deposition tools (three thermal, one e-beam, one sputterer), contact lithography (front- and back-side alignment), converted SEM e-beam lithography, focused ion beam, and numerous monitoring tools (FESEM, spectroscopic ellipsometer, contact profilometer, 4-point probe, microscope with image capture, etc.). We are also in the process of procuring a state-of-the-art e-beam lithography system with mask making capability, and nanoimprint lithography.

## Technical Contacts:

E. M. Vogel  
G. Henein



Figure 1. The NIST AML Nanofab silicon Reactive Ion Etcher.

The NF will be operated as a shared access user facility. This means that the staff of NIST and its partners, subject to provisions, training, and user fees, will be permitted to independently operate the equipment (Fig. 2). The tools will be operated in a manner such that a wide variety of materials can be processed. The facility will be directed by NIST's Semiconductor Electronics Division. Unlike other nanofabs, the NIST AML nanofab is unique in that it is located next to the most advanced metrology tools in the world, and its

focus will be on fabricating nanoscale structures necessary for metrology and standards in support of the semiconductor industry, nanotechnology, biotechnology, and homeland security.



*Figure 2. A user in the NIST AML Nanofab.*

**DELIVERABLES:** Facility fully operational by 1Q 2006.