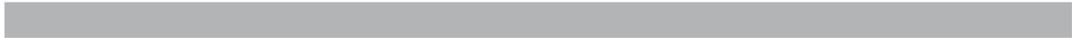


SYSTEM DESIGN AND TEST METROLOGY PROGRAM

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution pose additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.



METROLOGY FOR SYSTEM-ON-A-CHIP (SoC)

GOALS

One of the key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry is the development of measurement methods and standards for characterizing embedded-sensor (ES) Virtual Components (ES-VCs), a critical class of building blocks from which SoCs are developed. The goal of this project is to promote and support the development of hardware and software standards for specifying embedded-sensor (ES) virtual-components (VCs) compatible with the System-on-a-Chip (SoC) integration methodology used for digital IC design.

This NIST effort will enable ES-VCs to be included in SoC CAD libraries and enable integration of ES-VCs with the existing digital VCs used ubiquitously by industry to design large ICs. The methods and standards developed as a result of this work will be essential for the realization of integrated, low-cost, smart homeland security and environmental sensor systems. One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs including MEMS-based (MicroElectroMechanical System) VCs into SoCs.

The project activities include: multi-technology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ES-VCs compatible with digital methodologies, testing standards, verification standards and high-level models of system components. The NIST MEMS-based integrated gas-sensing VC is used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies is used to facilitate the adoption of these MT-VCs into new Homeland Security and Industrial applications.

CUSTOMER NEEDS

Recent advances in high density CMOS integration and the ability to co-integrate MEMS-based sensor devices enables cost effective complex system designs fabricated on a single chip. The need for standards arises when the system-on-a-chip is designed using IP (Intellectual Property) cores from multiple vendors. These cores must be compatible for design success, thus demanding standards in the area of interoperable interfaces, models and verification strategies for multi-technology SoC designs.

The SoC design challenges include managing increasing system complexity, achieving system-level verification, and bridging the separate disciplines of system architecture and chip design. These challenges are being overcome with the use of platform-based design approaches that emphasize design reuse, i.e. the development of ES-VCs that can be used as cost-effective building blocks for SoC devices, and standards for ES-VC IP interoperability with the SoC design flow.

The direct customers for this infrastructure building will be the makers of system design software, ES-SoC IP designers, SoC manufacturers and systems designers. This is generally recognized by the chip designers, manufacturers, and EDA tool developers:

“What is the most recent development that promises to truly enable a system on a chip? It is the ability to combine CMOS and MEMS structures into one process flow.”

Randy Frank and Dave Zehrbach, Motorola, in *Sensors Online*, 1998

“Definitely, System-on-a-chip is the driving paradigm in our space, and there are some fundamental differences in culture and engineering mentality as well as some new technical skills that need to be developed in engineering. At the highest level, system-on-a-chip implies that you need to think like a system designer but implement like a chip designer, and those traditionally have been different disciplines...”

Shane Robison, Executive Vice President of Engineering, Cadence Design Systems, Inc. EDAcade.com

TECHNICAL STRATEGY

1. To successfully develop ES-VCs for SoC design methodology, the first step in this multi-step process is to develop the ability to make the ES-VC devices via a standard CMOS compatible process. To exercise this capability we have chosen a MEMS microhotplate based embedded gas-sensor, including operational amplifiers, decoders, and an analog-to-digital converter (ADC) to process the data.
2. The second step is to make ES-VCs compatible with the standard digital SoC design methodology. This approach will require ES-VC to

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“... SoC is the driver for convergence of multiple technologies not only in the same system package but also potentially in the same manufacturing process.”

The International Technology Roadmap for Semiconductors, 2003.

incorporate digital interface circuitry and to have the DFT/BIST (Design For Test/ Built-In Self Test) functionality required by SoC standards. To facilitate this approach we will develop methodologies and standards for adding digital shells to ES-VCs and demonstrate them on the gas-sensor VC described above.

DELIVERABLES: Develop methodologies for designing digital interface shell functionality for ES-VCs and demonstrate their viability via our microhotplate gas-sensor technology. 4Q 2005

3. The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level models (in SystemC/HDL) exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ES-VCs is at best poorly developed. To address this need, high-level models are being developed for ES-VCs using Analog and Digital Hardware Description Languages and higher-level system description languages such as SystemC. We are also developing methodologies to validate these models. The digital systems industry has standards set by organizations such as OCP-IP, VSIA and OSCI to foster large-scale interchange and interoperability of modular digital IP, and we believe that such standards in ES-VC field are a key factor for the growth of an ES-VC IP industry.

DELIVERABLES: Develop high-level models for microhotplate gas-sensor ES-VCs to facilitate the development of standards for multi-technology SoC top-down design. 2Q 2006

4. Synthesis process is well defined for the digital SoC design and is well supported by a large number of design libraries. Currently the libraries, methodology, and standards for ES_VC synthesis do not exist. We are developing standards and metrologies for ES-VCs that will be compatible with standard digital synthesis tools.

DELIVERABLES: Develop methodology and standards to allow ES-VC to be synthesized by standard MT- synthesis tools and demonstrate their viability via our microhotplate gas-sensor VC. 4Q 2007

5. Scaling digital circuitry is a key capability used by digital designers to reduce costs and ensure compatibility with different fabrication technologies. Since most systems that would use ES-VCs will be predominantly digital, it is important that there be an equivalent scaling ca-

pability for the ES-VCs. To address the need for scaling ES-VCs, we are developing metrologies for digital-compatible scaling processes.

DELIVERABLES: Develop methodologies and standards for an equivalent ES-VC scaling approach and demonstrate its viability via our microhotplate gas-sensor technology. 4Q 2006

6. The testability of ES-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use BIST techniques. To facilitate this approach we will develop methodologies and standards for adding BIST to ES-VCs and interface with them via the digital shell.

DELIVERABLES: Develop methodologies for built-in self test of ES-VC devices and demonstrate their viability via our microhotplate gas-sensor technology. 2Q 2007

NIST is a natural home for this work because NIST has advanced measurement capabilities across the spectrum of sensor technologies.

ACCOMPLISHMENTS

- A monolithic micro-gas-sensor system was successfully designed and fabricated in a standard 1.5 μm CMOS process. The gas-sensor system incorporated an array of four microhotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SnO_2) as a sensing material. Digital decoders selected individual elements of the sensor array and an operational amplifier monitored sensing film conductance. Detection of gas concentrations in the 100 parts-per-billion range was achieved. This represented an improvement in sensitivity of two orders of magnitude over existing MEMS-based microhotplate gas-sensors (see Fig. 1).

- Investigated existing and emerging SoC design methodologies, and adapted digital SoC design tool-flow to enable integration of mixed-signal MEMS VCs.

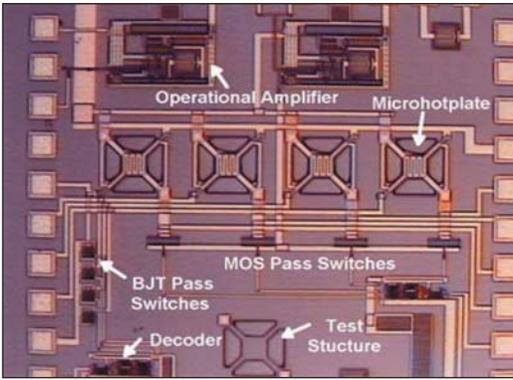


Figure 1. Micrograph of gas-sensor system to be used as demonstration vehicle.

- A four element gas-sensor VC was successfully designed, fabricated and electrically characterized to demonstrate that the design approach was compatible with SoC design methodology. The performance of the 8-bit ADC exceeded the gas-sensor VC design requirements (see Fig. 2).

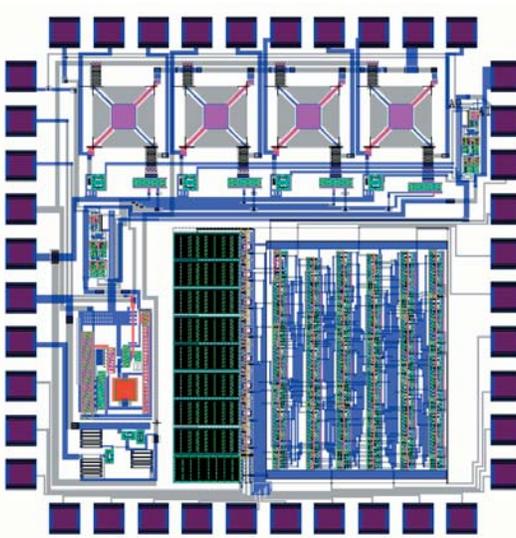


Figure 2. Layout of the four element gas-sensor VC with analog-to-digital control.

- Electrostatic discharge (ESD) protection structures were added to the gas-sensor and successfully tested. These ESD test structures are based on multi-finger thyristor-type devices and are designed to achieve optimum performance and reduced area (see Fig. 3).

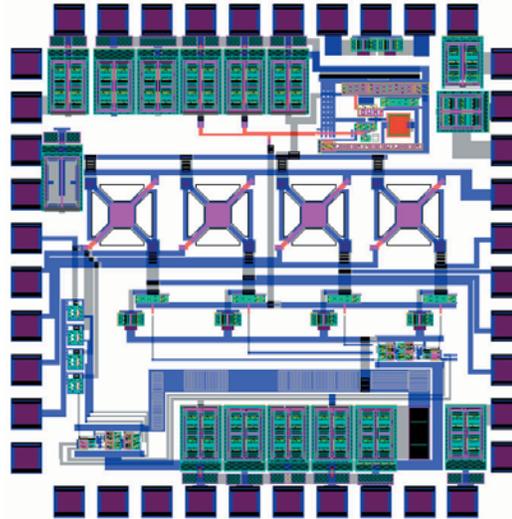


Figure 3. Layout of the four element gas-sensor VC with electrostatic discharge (ESD) protection circuitry.

- A new post-process etching technique was developed to integrate MEMS devices with standard submicron CMOS processes and a new microhotplate design that scales with standard CMOS structures and voltage levels. This will enable co-integration of MEMS sensor devices with high density submicron digital systems using cost effective standard CMOS foundries. The submicron gas-sensor test chip was characterized. Characterization data showed the new scalable microhotplate will provide the temperature required for gas-sensor operation at 3.3 V (see Fig. 4).

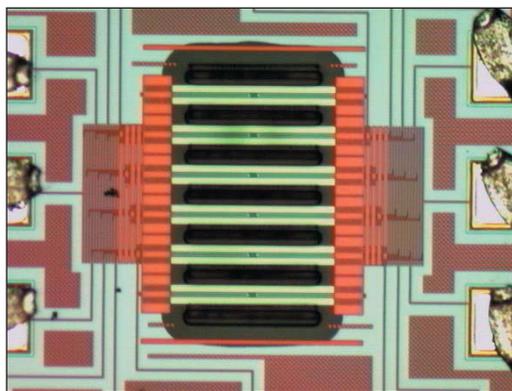


Figure 4. New microhotplate design implemented in standard submicron CMOS technology.

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BIOELECTRONICS METROLOGY

GOALS

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal over the next five years is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it to study neural (retinal) single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

CUSTOMER NEEDS

Cell-based assays are a primary tool used by the pharmaceutical industry to measure therapeutic drug efficacy and cytotoxicity. These time-consuming and labor-intensive assays currently involve millions of cells in each culture reservoir. This leads to some inherent measurement biases since the collective response only represents the average for the whole population and, for example, cells at different stages of development will respond differently to stimuli. A true paradigm shift is to utilize micro- and nanofabrication technologies to perform these experiments on single cells or small cell clusters in continuous flow microfluidic systems with integrated microsensors and MEMS. Single-cell assays will isolate the parameters affecting cell response and allow the various subpopulations present in bulk cultures to be distinguished. Single-cell assays, when multiplexed, will allow for more rapid identification of drugs and drug targets.

TECHNICAL STRATEGY

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the *in vitro* measurement systems, developing stable and drift-free electrodes for accurate measurements, in varied buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid *in vitro* environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We will focus our initial research efforts on the study of retinal (neuronal) cells and will later progress to other cell systems.

DELIVERABLES:

Develop an array of micro-electrochemical cells and methods to pattern cells on the array for single-cell electrochemical measurements.

Technical Contacts:

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J. J. Kasianowicz
D. R. Reyes
B. J. Polk

A cellular microenvironment for sustained single cell growth and development;

Microfluidic and microelectronic components on a single platform for delivering precise chemical stimuli to single cells;

Demonstrate the capability to manipulate and stimulate cells within the microenvironment using fluidic, electronic and optical techniques;

New methods for temperature regulation and electronic detection using microwave technologies;

Continuous monitoring of cell growth, development and viability in the presence and absence of therapeutic drugs and chemical toxins.

ACCOMPLISHMENTS

■ We developed a method to adhere retinal cells on micropatterned polyelectrolyte multilayer (PEM) lines adsorbed on poly(dimethylsiloxane) (PDMS) surfaces using microfluidic networks. PEMs were patterned on flat, oxidized PDMS surfaces by sequentially flowing polyions through a microchannel network that was placed in contact with the PDMS surface. Polyethyleneimine (PEI) and poly(allylamine hydrochloride) (PAH) were the polyions used as the top layer cellular adhesion material. The microfluidic network was lifted off after the patterning was completed and retinal cells were seeded on the PEM/PDMS surfaces. The traditional practice of using blocking agents to prevent the adhesion of cells on unpatterned areas was avoided by allowing the PDMS surface to return to its uncharged state after the patterning was completed. The adhesion of rat retinal cells on the patterned PEMs was observed 5 hours after seeding. Cell viability and morphology on the patterned PEMs were assayed. These materials proved to be nontoxic to the cells used in this study regardless of the number of stacked PEM layers. Phalloidin staining of the cytoskeleton revealed no apparent morphological differences in retinal

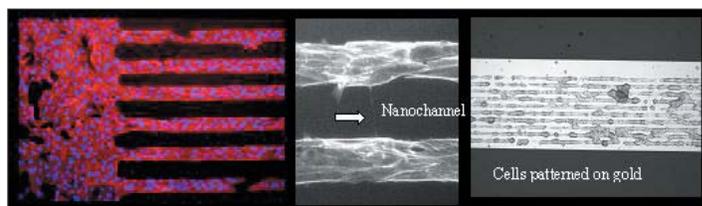


Figure 1. The left and center panels are images of R28 cells retinal patterned using polyelectrolyte multilayers lines adsorbed on poly(dimethylsiloxane). The center panel shows a nanochannel that was spontaneously formed by the cells. The right panel is an image of cells patterned on a gold surface using the polyelectrolyte multilayers.

cells compared with those plated on polystyrene or the larger regions of PEI and PAH; however, cells were relatively more elongated when cultured on the PEM lines. Cell-to-cell communication between cells on adjacent PEM lines was observed as interconnecting tubes containing actin that were a few hundred nanometers in diameter and up to 55 μm in length. This approach provides a simple, fast, and inexpensive method of patterning cells onto micrometer-scale features.

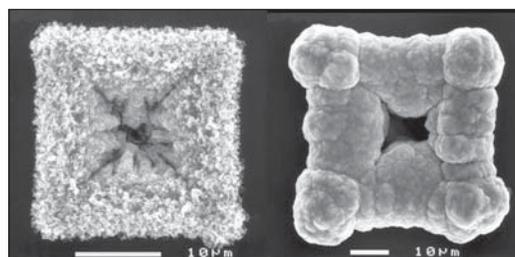


Figure 2. SEM images of two silver nanopores formed by electroplating on micromachined silicon micropores.

■ We developed a method to create nanofluidic restrictions by electroplating silver on micrometer scale pores. Electrodeposition of silver was investigated as a fabrication tool for constricting large ($10^3 \mu\text{m}^2$) vias in silicon substrates while leaving a small opening in the center of the via. Silver reduction from ammoniacal silver nitrate was studied at electrodes of novel geometry (*i.e.*, the edge of the vias) with respect to reduction potential, reduction pulse type, and pulse duration. A variety of crystal nucleation and growth patterns was observed and characterized by scanning electron microscopy. It was found that electroplated silver occluded the vias to leave open areas of less than $1 \mu\text{m}^2$. Such occlusions might be used as restrictions in microfluidics systems, forming a type of solid-state micropore or nanopore.

■ A method for fabricating Ag/AgCl planar microelectrodes for microfluidic applications is presented. Micro-reference electrodes enable accurate potentiometric measurements with miniaturized chemical sensors, but such electrodes often exhibit very limited lifetimes. Our goal is to construct Ag/AgCl microelectrodes reliably with improved potential stability that are compatible with surface mounted microfluidic channels. Electrodes

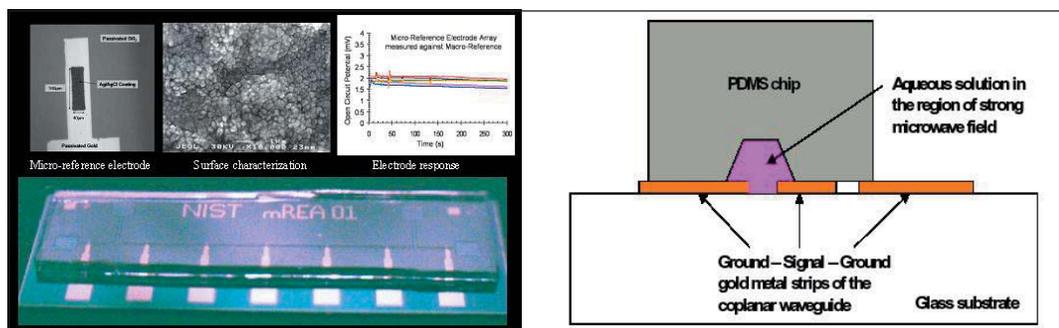


Figure 3. Photographs (left panel) of the NIST micro reference electrode array (mREA) and close-up photo of an Ag/AgCl planar microelectrode, surface, and test. The right panel is a drawing of a fluidic microwave heating assembly showing a gold coplanar transmission line patterned on glass with a poly(dimethylsiloxane) microchannel bonded over it.

with geometric surface areas greater than or equal to 100 square micrometers were fabricated individually and in an array format by electroplating silver, greater than one micrometer thickness, onto photolithographically patterned thin-film metal electrodes. The surface of the electroplated silver was chemically oxidized to silver chloride to form Ag/AgCl microreference electrodes. Characterization results showed that Ag/AgCl microelectrodes produced by this fabrication method exhibit increased stability compared with many devices previously reported. Electrochemical impedance spectroscopy allowed device specific parameters to be extracted from an equivalent circuit model, and these parameters were used to describe the performance of the microelectrodes in a microfluidic channel. Thus, stable Ag/AgCl microelectrodes, fabricated with a combination of photolithographic techniques and electroplating, were demonstrated to have utility for electrochemical analysis within microfluidic systems.

■ Rapid temperature cycling of fluids is essential for increasing the throughput of chemical and biochemical processes and chemical synthesis such as polymerase chain reaction (PCR). In micro total analysis systems (μ TAS), temperature cycling is typically implemented by external heating blocks or by integrated microresistive heating elements (microreactors). In this paper, a new approach for temperature cycling of microfluidic systems is presented that is based on delivering microwave heating energy using a microwave transmission line. A microwave coplanar waveguide is integrated with a surface mounted elastomeric microfluidic channel. We demonstrate that the microwave signal can be tuned to most effectively deliver the heat to the fluid at a frequency of 18 GHz (in agreement with theory) independent of the ionic strength of the

solution. This approach will have application to microwave assisted chemistries which have recently been shown (in macro-scale devices) to have several advantages over conventional resistive heating approaches. These advantages include the ability to deliver heat directly to the fluid (and not to the surrounding medium), requiring lower temperatures to implement a chemical reaction and exhibition of more uniform heating profiles. This paper suggests that those advantages can also be realized in a microfluidic format.

■ We have integrated electrodes within microfluidic devices to carry out AC dielectrophoresis. In this trapping technique, electric fields polarize cells inducing electrostatic forces, which trap the cells against the electrode edges. We have been able to trap cells suspended from bulk cultures within microchannels when flowed past integrated, energized electrodes. We have observed that more than 85 % of cells passing the electrodes were trapped. On the other hand, when electrodes were deactivated, about 70 % of the cells were subsequently detached by solution flow. Deposition of PEMs on the electrodes renders an adhesion layer to further cell attachment. Trapping experiments carried out after PEMs were deposited over the electrodes showed that all immobilized cells remained adherent after the electrodes were deactivated. We have been using AC dielectrophoresis to array cells within a microfluidic channel perpendicular to flow.

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AT-SPEED TEST OF DIGITAL INTEGRATED CIRCUITS

GOALS

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes, develop scanning probe microscopes (SPMs) capable of precisely positioning field probes above the surface of the integrated circuit, and push the current on-chip sampling technologies now being explored by the industry.

CUSTOMER NEEDS

In the device debug and characterization world, at-speed functional and analog test will continue to serve as a primary vehicle for root cause of design process errors and marginalities (2003 ITRS Test and Test Equipment Section, page 1). Traditional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use high-impedance probes, non-contact probes, atomic-force microscopes, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

The need for noninvasive waveform measurements in silicon integrated circuits is discussed in the Test and Test Equipment section, pages 1-5, 2001 (International Technology Roadmap for Semiconductors).



Figure 1. Universal test bed for electric and magnetic field probing on a nanoscale.

TECHNICAL STRATEGY

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we are constructing a universal SPM test bed for these probes (Fig. 1). We will then apply our characterization procedures to miniature SPM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we will tie our metrology back to fully characterized electro-optic sampling measurements.

NIST also is working on methods for calibrating and correcting imperfections in waveform measurement equipment that cause distorted or blurred measurements. These effects include instrument response, impedance mismatch, multiple reflections, dispersion, time-base distortion, jitter, and drift. After calibration and correction, the measurement has an improved fidelity and is traceable to fundamental physical principles. For example, Fig. 2 shows measurement of a short bit sequence, transmitted at 10 Gbit/s, and plotted in the form of an eye pattern. Before correction for time-base distortion and jitter (caused by the

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P. Kabos
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P. Hale

“As electronic devices shrink into the nano-meter size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before.”

*Travis M. Eiles, Ph.D.
Intel Corp.*

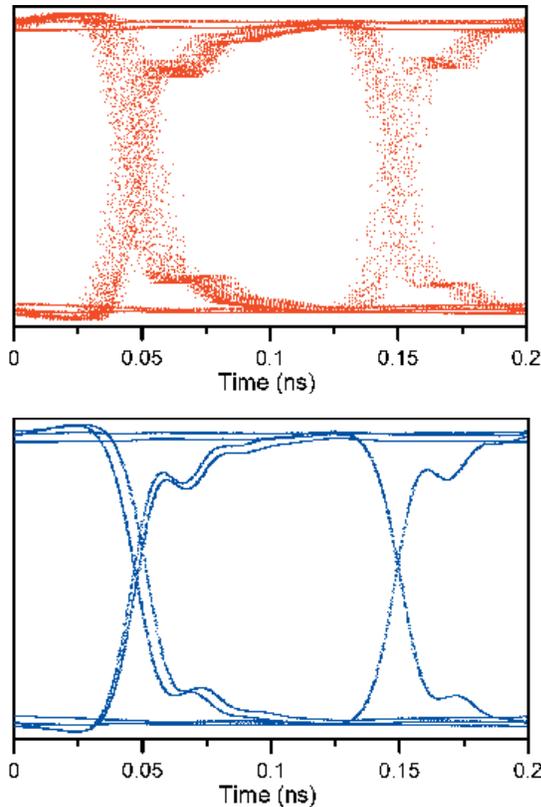


Figure 2. Measurement of 10 Gbit/s eye pattern before (a) and after (b) correction for oscilloscope time-base distortion and jitter using NIST developed techniques.

oscilloscope) the eye pattern is blurred while after correction fine features in the eye pattern, such as pattern-dependant jitter, are clearly revealed. Traceability for frequency response is provided to 110 GHz (in coax) and beyond (on wafer) through the NIST electro-optic sampling system.

DELIVERABLE: Test high-impedance probe with single-step 200 GHz EOS calibration. 2Q 2005

DELIVERABLE: Mismatch corrected photodiode impulse response calibration, traceable to the EOS at the 1.00 mm coax plane with covariance matrix that enables point by point time- and frequency-domain uncertainty analysis. 3Q 2005

DELIVERABLE: Measure the magneto-mechanical response of sensors integrated with fiber optic cantilever probe. 4Q 2005

ACCOMPLISHMENTS

- We have designed and tested a prototype sinusoidal waveform standard.
- We have constructed a high-speed electro-optic sampling system.

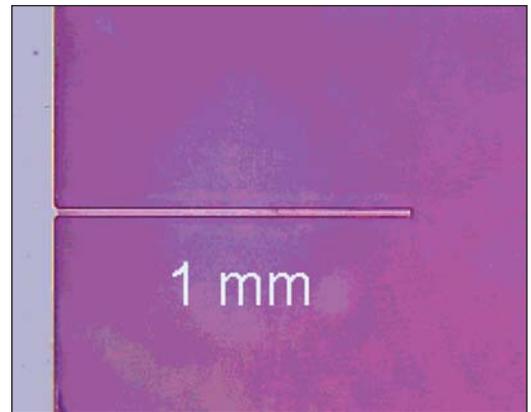


Figure 3. A 1 mm long dielectric bimaterial cantilever AFM probe fabricated at NIST for noninvasively measuring local microwave power.

- We have developed, fabricated and tested a noninvasive AFM scanning probe for measuring local microwave power (see Fig. 3).
- We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements (see Fig. 4).
- We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.
- We have constructed an SPM universal test bed.
- We have demonstrated a calibrated measurement of an on-wafer pulsed waveform up to 200 GHz using electro-optic sampling.

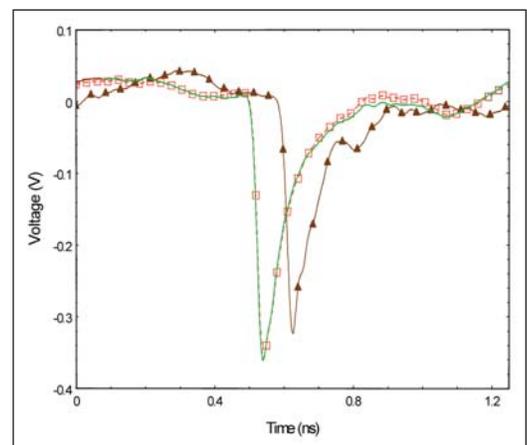


Figure 4. Waveform comparison at the tip of a commercial high-impedance probe. The red curve marked with red squares is the expected waveform. The brown curve marked with triangles is the measured waveform. The green curve is the measured waveform after correction by the new NIST algorithm.

- We have demonstrated a method for correcting oscilloscope timebase jitter, drift, and distortion.

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P. D. Hale, C. M. Wang, D. F. Williams, K. A. Remley, and J. Wepman, "Compensation of random and systematic timing errors in sampling oscilloscopes," submitted to IEEE Trans. Instrum. Meas.

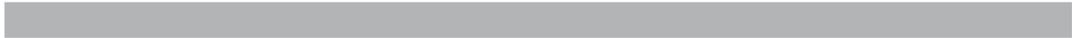
D.F. Williams, P.D. Hale, T.S. Clement, and J.M. Morgan, "Calibrated 200 GHz Waveform Measurement," IEEE Trans. Microwave Theory and Tech., April, 2005.

P. Kabos, H. C. Reader, U. Arz, and D. F. Williams, "Calibrated waveform measurement with high-impedance probes," IEEE Trans. Microwave Theory and Tech., February 2003.

M. D. Janezic, D. F. Williams, V. Blaschke, A. Karamcheti, and C. S. Chang, "Permittivity characterization of low- κ thin films from transmission-line measurements," IEEE Trans. Microwave Theory and Tech. January 2003.

T. S. Clement, P. D. Hale, D. F. Williams, and J. M. Morgan, "Calibrating photoreceiver response to 110 GHz," 15th Annual Meeting of the IEEE Lasers and Electro-Optics Society Conference Digest, Nov. 10-14, 2002, Glasgow, Scotland.

Albrecht Jander, John Moreland, and Pavel Kabos, "Dielectric micromachined calorimeter probe for high resolution microwave power measurements based on ferromagnetic resonance," 15th IEEE Int. Conf. on MicroElectroMechanical Systems, Jan. 20-24, 2002, Las Vegas, Nevada.



THERMAL MEASUREMENTS AND PACKAGING RELIABILITY

GOALS

Provide the microelectronics packaging industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens that present a reliability concern to the manufacturer or end-user. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical meetings. This system contributes toward achieving our third and primary goal—providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allow us to refine the techniques to make them optimally beneficial to industry, and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, which is essential for technology transfer.

Overcoming thermal limitations has recently become a major issue in CMOS-based microelectronic circuits because: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (*e.g.*, SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in the interconnects. To address these issues, reliable methods for measuring the temperature distribution in ICs and power devices are required.

A broad range of temperature measurement techniques are investigated by this project and several unique temperature measurement system requirements have been identified and demonstrated by NIST. High speed transient thermal imaging methods are being developed for measuring localized heating effects at the semiconductor chip surface. This enables the measurement of transient heating events such as burst operation of IC Functional Unit Blocks (FUBs)

and enables the measurement of transient current constriction failure events in RF and high power devices. Additionally, methods are being developed to evaluate the heat transfer across package layer interfaces using high-speed temperature sensitive parameter (TSP) measurements. This is important for in-situ measurement of heat transfer performance degradation after various levels of thermal stress such as thermal cycling and thermal shock.

CUSTOMER NEEDS

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging are many and display a variety of thermal responses that are not always compatible. This makes interfaces particularly vulnerable to thermomechanical fatigue failures. The program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry.

The need to measure operating temperature of a semiconductor device can be divided into the following four broad categories: 1) predicting reliability or operating life of device, 2) measuring material/device thermal properties *in-situ*, 3) confirming or determining the operating limits or thermal performance of a device, and 4) validating thermal models for device, chip and system performance. Thermal measurements on small, <10 μm structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer information at interfaces, such as those seen at solder/intermetallic interfaces and Direct Bonded Copper (DBC) isolation layer is needed for modeling of future package designs.

Temperature measurements for microelectronic devices are more important today than they ever have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to “Moore’s Law.” Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate

Technical Contacts:

A. J. Slifka
A. R. Hefner

“I am writing to let you know that NIST has been of great assistance to Cenymex Corporation, one of our portfolio companies. This portfolio company has developed a novel material. Dr. Andrew Slifka at NIST was able to provide the company with thermal measurements that are critically important to Cenymex as it approaches potential customers. It is great to have NIST in the community as a resource to companies like Cenymex.”

*Tim Connor
Sequel Venture Partners*

and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

Measurement of localized and transient heating is also becoming increasingly important in high performance ICs as it is becoming prohibitive to remove the heat that would be dissipated if the entire IC was operated continuously at the full power density level. System techniques that dynamically operate all or part of the chip at reduced power, such as dynamic voltage scaling or clock gating, require experimental evaluation of the rapid transient heating and thermal diffusion from locally heated FUBs. System level power reduction strategies are generally recognized by the ITRS 2003 as necessary for the continual advancement of electronic systems at a rate consistent with "Moore's law."

"The high-performance market sector has experienced a dramatic increase in power over the different generations.... In addition to managing total chip power requirements in excess of 100 Watts, solutions to manage power density and internal hot spots are necessary." ITRS 2003

"Achieving the necessary reliability: New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key." 2003 ITRS: one of the five "Difficult Interconnect Challenges through 2009

"Integration of new processes and structures, including interconnects for emerging devices: Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects." Novel/active devices may be incorporated into the interconnect. 2003 ITRS: one of the five "Difficult Interconnect Challenges beyond 2009

The maximum junction temperatures for chip operation are shown in tables 93 a and b of the ITRS Assembly and Packaging section. Issues concerning the poor thermal conductivity of low- κ dielectrics is discussed on page 34 of the Reliability section.

TECHNICAL STRATEGY

1. Our established program in infrared (IR) (thermal) microscopy and our developing techniques in scanning thermal microscopy, utilizing

the AFM (atomic force microscope), have much to offer the microelectronics industry. We have been approached by industry with requests for aid as simple as "How high are the temperatures in this MCM (multichip module) during service" to as challenging as "What is the interfacial thermal resistance of an alloy/intermetallic interface." The first was answered using the IR microscope; the second has yet to be answered.

We have just completed our fourth year of applying thermal conductivity measurements using the IR microscope to the problem of packaging reliability, and have engendered great interest from the Advanced Embedded Passive Technology (AEPT) Consortium. As thermal conductivity measurements are one of the most sensitive indicators of metal purity, likewise they are one of the most sensitive indicators of interfacial integrity. A minute increase in interfacial thermal conductivity is the first indication of the microcracks and fissures that ultimately may result in failure.

DELIVERABLES: Scanning Probe Microscope (SPM) thermal measurement of aluminum interconnect lines. 2Q 2005 Publication of thermal and electrical measurements. 4Q 2005

2. As the size of packages gets smaller, heat removal becomes a more significant problem. The SPM is being used to develop a technique to measure thermal conductivity of thin films for application to metal interconnect lines. The technique also will be able to measure interfacial thermal resistance between coatings and substrates. The theoretical work on this development is being done in collaboration with Dr. Kevin Cole of the University of Nebraska.

DELIVERABLES: Report via the literature, on measurements of a model film, such as gold or different substrates. 3Q 2005

3. Carbon nanotubes have potential in heat-removal applications and in wear applications. Thermal properties show great promise in this area, if production issues can be addressed. We are currently measuring carbon nanotubes made from different inexpensive processes to determine if heat removal applications are economically and technologically feasible.

DELIVERABLES: Measure interfacial thermal resistance of carbon nanotube-covered copper and baseline copper materials. 2Q 2005

4. Interfacial thermal resistance measurement of the interface between solders and intermetallics supplies a piece to the puzzle of thermal dissipation from high-density packages. The small size of current and future solder bump processes requires higher spatial resolution thermal measurement methodologies.

DELIVERABLES: Measure interfacial thermal resistance of interfaces in in-house and industrial solder alloys. 4Q 2005

5. High speed temperature sensitive parameter (TSP) measurements are required for in-situ evaluation of the heat transport through the interface of multi-layer package systems. Recently NIST developed a high speed transient thermal impedance system using a TSP for multi-chip power modules. This enables assessment of die attach and DBC isolation attach degradation after thermal cycling and thermal shock stress. This system also enables validation of electro-thermal device models needed for electrical and thermal system design

DELIVERABLE: Perform thermal cycling and thermal shock stress on DARPA Wide-Bandgap High Power Electronics program devices and American Competitiveness Institute ManTech devices. Use unique NIST high speed, high current TSP system to evaluate die attach and DBC attach integrity before and after thermal stress. 4Q 2006

6. A limitation of commercially available infrared (IR) thermal imaging systems is their inability to make high speed transient measurements. NIST has modified a commercial IR system to enable measurement of high speed temperature maps of the chip surface with 1 μ s time resolution and 15 μ m spatial resolution. The new system permits the measurement of the chip heat source distribution before the heat diffuses to surrounding regions and enables the measurement of transient heating events such as burst operation of IC FUBs and enables the measurement of transient current constriction failure events in RF and high power devices.

DELIVERABLE: Apply high speed thermal imaging system to characterize localized dynamic heating of FUBs in advanced digital integrated circuits. 2Q 2006

ACCOMPLISHMENTS

■ Completed analysis of measurements on industrial specimens from AEPT using thermal SPM, laser-heated IR microscopy, and Joule-heated IR microscopy. Reported results at GOMACTech 2004 Conference.

■ Thermal measurements have continued on three similar embedded resistor specimens. One specimen each is being measured using laser-heated IR microscopy, Joule-heated IR microscopy, and thermal SPM. The results were analyzed and the techniques compared. All three specimens have been thermally cycled 18 times, and data analysis shows consistency between the techniques. Figure 1 shows relative thermal resistance data as a function of thermal cycling from Joule-heated measurements.

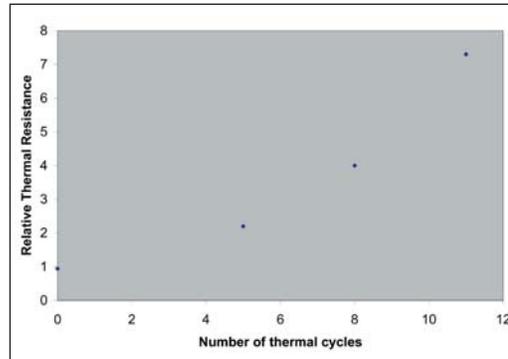


Figure 1. Joule-heated IR microscopy measurements showing relative thermal resistance as a function of thermal cycling.

■ Development of a technique for measuring the thermal conductivity of thin films using the SPM has begun. Most films used in electronics and electronic packaging are so thin that a measurement using even the thermal SPM would be primarily a measurement of the substrate material. With collaboration from Dr. Kevin Cole of the University of Nebraska, work has begun on a theoretical treatment of the data to allow measurement of thin films and the interfacial thermal resistance between the film and substrate. One application for this technique is measurement of thermal properties of interconnect lines. Measurements have begun using a model system, consisting of gold films of various thickness evaporated onto glass substrates. Figure 2 (pg. 196) shows thermal measurement data on films of differing thickness.

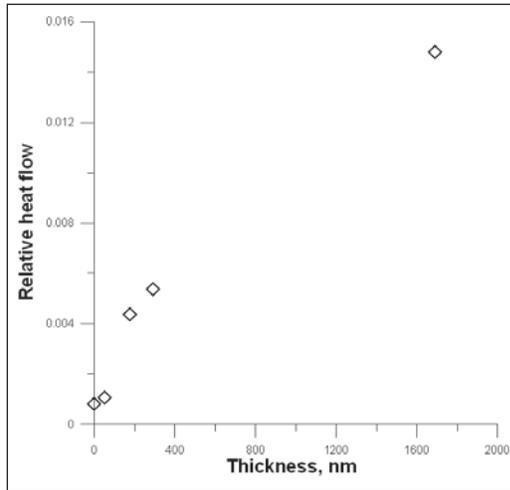


Figure 2. Thermal measurement data on thin gold films on glass substrates.

■ We have been approached by Cenymmer Corporation to make thermal and other measurements on a diamond-like carbon coating that they manufacture. Since these coatings are typically around a micron thick, the thermal SPM is a good tool for this measurement. Cenymmer also is interested in interface materials to allow adhesion of diamond-like carbon coatings to various substrates. This work fits well with our thin-film research, providing specimens with different, controlled interfaces to help solve the problem of analyzing thermal data on thin films and even thinner adhesion layers. Figure 3 shows a measurement result from one of their coatings.

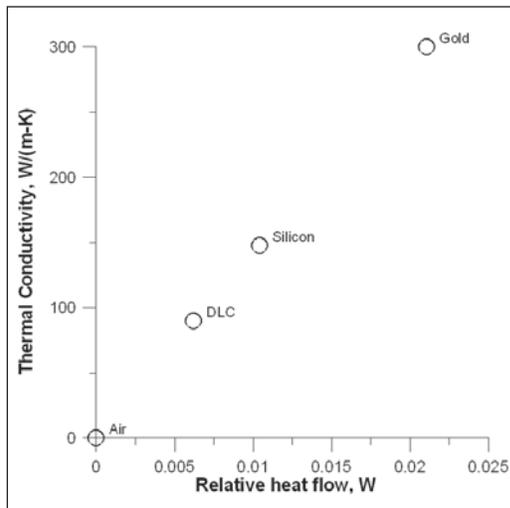


Figure 3. Thermal conductivity measurement of a 1.9 μm thick DLC coating and the comparative measurements of known materials using the same setup.

■ Completed the development of the high speed transient thermal imaging system. The acquisition and data analysis capabilities of this system have been extended to include a burst method and to allow frames from different transient movies to be compared more readily. All functions have been tested and verified.

■ Sequences of thermal images were taken at stages of progressive degradation on SiC diodes, starting with virgin diodes and progressing with the same diodes showing degraded electrical performance. The results show that the current is relatively uniform before degradation and that only 1 % of the chip is conducting all of the current after degradation.

■ We have developed a method to measure the high-speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, V_{GS} , at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter. Under these circumstances, variations in V_{GS} result from equal changes in the threshold voltage. The method is used to validate and extract short-time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module). Under the measurement conditions used, there are concerns about the sharing of current between the chips in the package, but by taking these into account, excellent agreement is obtained between the measured and simulated temperatures (Fig. 4). The module is shown in Fig. 5a and 5b.

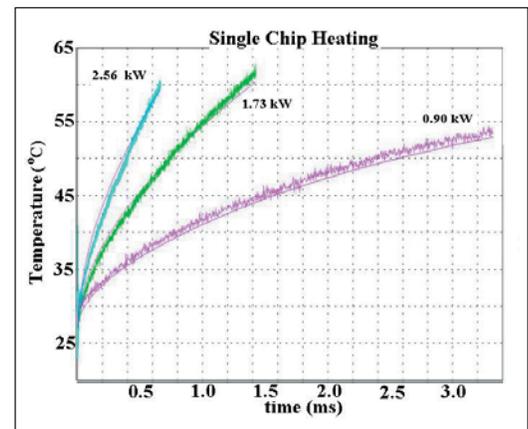


Figure 4. Electrically measured and computer simulated measurement of the temperature of IGBT chip in a power module.

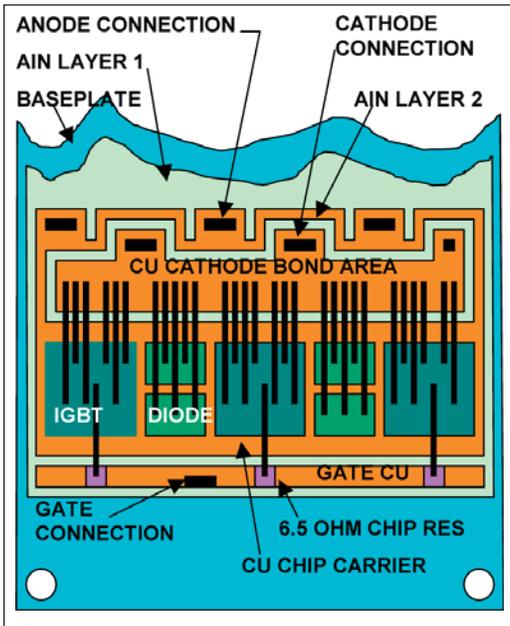


Figure 5a. Drawing of the layout of the IGBT chips within the module.

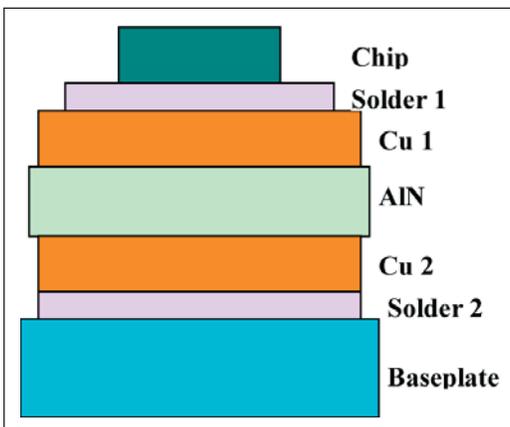


Figure 5b. Drawing of the vertical structure in the power module from one of the chips at the top to the baseplate at the bottom.

- Applied the new high-speed heating response measurement and modeling method to commercial high power IGBT half bridge module, commercial six-pack IGBT module, and prototype NSF Center for Power Electronic Systems Module. Electro-thermal simulations of a full three-phase inverter have been successfully performed, and a paper was completed and will appear at the IEEE Power Electronics Specialist Conference in June 2005.

- An invited presentation, “Semiconductor Device Temperature Measurements,” was presented at the 20th IEEE Semiconductor Thermal Measurement and Management Symposium

(SemiTherm) in March 2004. The talk covered the basic physical phenomena of a wide variety of temperature-sensitive devices and material parameters that have been used for measuring chip-level temperatures. The temperature, spatial, and temporal resolutions of each of the three generic measurement types (electrical, optical, and contacting) were emphasized. Power dissipation and excessive temperature have been identified as barriers to the continued shrinking and performance improvements for CMOS and beyond technologies. Perhaps the major issues with temperature measurements for advanced semiconductor chips and novel electronic structures are spatial and temporal resolution. Scanning thermal probes have been shown to have a spatial resolution between 30–50 nm, but they have a relatively slow time response and measurement interpretation is difficult due to the complexity of the physical contact between the probe and the specimen. Optical methods, such as thermoreflectance and Raman spectroscopy, potentially have picosecond time resolution, but they are diffraction limited in their spatial resolution typically to about 1 μm typically. There continues to be much interest in the development of methods for measuring chip temperatures with improved spatial and time resolution.

- Feasibility has been shown of measurements of electronic interconnect lines using the thermal SPM. We are now calibrating the response of the probe tip to temperature.

COLLABORATIONS

AEPT Consortium

DuPont: John Felten

MacDermid: Dennis Fritz

Merix: Bob Greenlee

MicroFab: Virang Shah

SAS Circuits: Richard Snogren, Matt Snogren

Colorado School of Mines: Ivar Reimanis, Saki Krishnamurthy, John Berger

University of Nebraska: Kevin Cole

Cenymex Corporation: Scott Joray

University of Maryland: Bruce Jacob

University of Maryland CALCE Electronic Products and Systems Center: Patrick McCluskey

American Competitiveness Institute (ACI), Navy ManTech center: Barry Thaler

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Slifka, A. J., Drexler, J. W., "Apparent Mobility of Interfaces in Integral Resistor Material," *Microscopy and Analysis*, pp.19-21 (January 2003).

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J. Rodriguez, Z. Parrilla, M. Veléz-Reyes, A. Hefner, D. Berning, J. Reichl, and J. Lai, "Thermal Component Models for Electro-Thermal Analysis of Multichip Power Modules," in *Conference Record IEEE Industry Applications Society Meeting*, pp. 234-241 (October 2002).

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Ortiz-Rodríguez, J. M., Hefner, A. R., Vélez-Reyes, M., and Gonzalez, J., "Electro-Thermal Modeling of the IPEM Generation II in SABER," *CPES Annual Industry Seminar*, April 28-29, 2002.

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